LECTURE NOTES ON

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Chapter 1 FIELD EFFECT TRANSISTORS

1.1   INTRODUCTION

The field-effect transistor (FET) is a three-terminal device used for a variety of applications that match, to a large extent. Although there are important differences between the two types of devices, there are also many similarities.

The primary difference between the two types of transistors is the fact that the BJT transistor is a *current-controlled* device as depicted in Fig. 1.1(a), while the JFET transistor is a *voltage-controlled* device as shown in Fig. 1.1(b). In other words, the current I_C in Fig. 1.1(a) is a direct function of the level of I_B. For the FET the current I will be a function of the voltage V_{GS} applied to the input circuit as shown in Fig. 1.1(b).
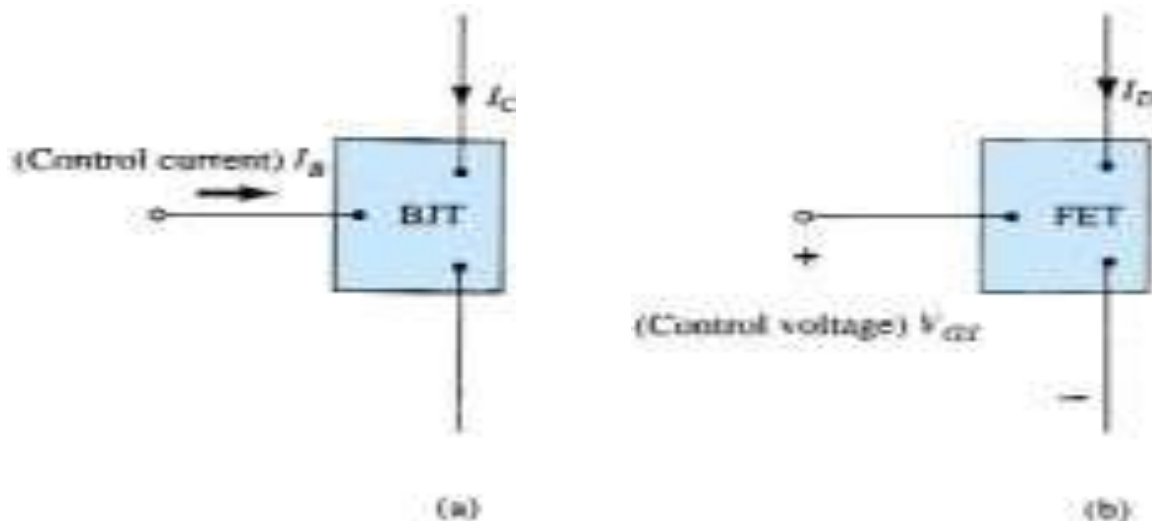

Fig. 1.1 (a) Current-controlled and (b) voltage-controlled amplifiers

In each case the current of the output circuit is being controlled by a parameter of the input circuit—in one case a current level and in the other an applied voltage. Just as there are *npn* and *pnp* bipolar transistors, there are *n-channel* and *p-channel* field-effect transistors. However, it is important to keep in mind that the BJT transistor is a *bipolar* device—the prefix *bi-* revealing that the conduction level is a function of two charge carriers, electrons and holes. The FET is a *unipolar* device depending solely on either electron (*n*-channel) or hole (*p*-channel) conduction.

The term field-effect in the chosen name deserves some explanation. For the FET an *electric field* is established by the charges present that will control the conduction path of the output circuit without the need for direct contact between the controlling and controlled quantities.

One of the most important characteristics of the FET is its *high input impedance.* At a level of 1 to several hundred mega ohms it far exceeds the typical input resistance levels of the BJT transistor configurations—a very important characteristic in the design of linear ac amplifier systems. On the other hand, the BJT transistor has a much higher sensitivity to changes in the applied signal. In other words, the variation in output current is typically a great deal more for BJTs than FETs for the same change in applied voltage. For this reason, typical ac voltage gains for BJT amplifiers are a great deal more than for FETs. In general, FETs are more temperature stable than BJTs, and FETs are usually smaller in construction than BJTs, making them particularly useful in *integrated-circuit (IC)* chips. The construction characteristics of some FETs, however, can make them more sensitive to handling than BJTs.

Two types of FETs are there: the *junction field-effect transistor* (JFET) and the *metal-oxide-semiconductor field-effect transistor (MOSFET).*
The MOSFET category is further broken down into depletion and enhancement types. The MOSFET transistor has become one of the most important devices used in the design and construction of integrated circuits for digital computers. Its thermal stability and other general characteristics make it extremely popular in computer circuit design.

1.2   CONSTRUCTION AND CHARACTERISTICS OF JFETs

The JFET is a three-terminal device with one terminal capable of controlling the current between the other two.
The basic construction of the *n*-channel JFET is shown in Fig. 1.2. Note that the major part of the structure is the *n*-type material that forms the channel between the embedded layers of *p*-type material. The top of the *n*-type channel is connected through an ohmic contact to a terminal referred to as the *drain (D),* while the lower end of the same material is connected through an ohmic contact to a terminal referred to as the *source (S).* The two *p*-type materials are connected together and to the *gate (G)* terminal. In essence, therefore, the drain and source are connected to the ends of the *n*-type channel and the gate to the two layers of *p*-type material. In the absence of any applied potentials the JFET has two *p-n* junctions under no-bias conditions. The result is a depletion region at each junction as shown in Fig. 1.2 that resembles the same region of a diode under no-bias conditions. A depletion region is that region void of free carriers and therefore unable to support conduction through the region. The drain and source terminals are at opposite ends of the *n*-channel as introduced in Fig. 1.2 because the terminology is defined for electron flow.
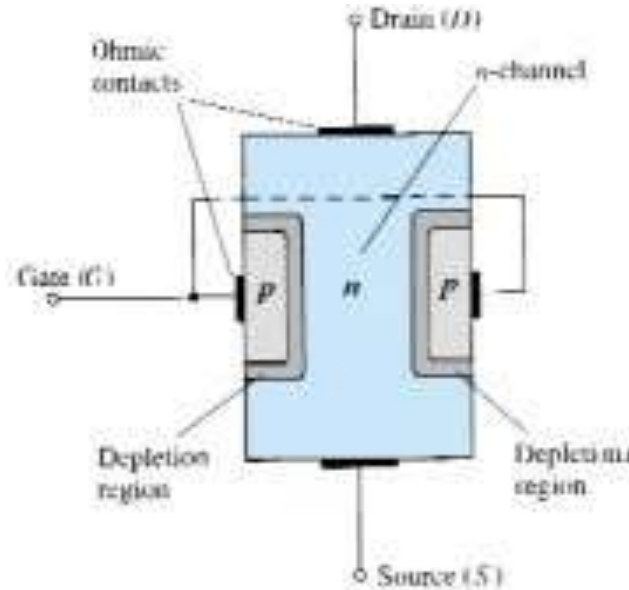
Fig 1.2 Junction field-effect transistor (JFET)

$V_{GS} = 0$ V, V_{DS} Some Positive Value

In Fig. 1.3, a positive voltage V_{DS} has been applied across the channel and the gate has been connected directly to the source to establish the condition $V_{GS} = 0$ V. The result is a gate and source terminal at the same potential and a depletion region in the low end of each p-material similar to the distribution of the no-bias conditions of Fig. 1.2. The instant the voltage V_{DD} ($= V_{DS}$) is applied, the electrons will be drawn to the drain terminal, establishing the conventional current I_D with the defined direction of Fig. 1.3. The path of charge flow clearly reveals that the drain and source currents are equivalent ($I_D = I_S$). Under the conditions appearing in Fig. 1.3, the flow of charge is relatively uninhibited and limited solely by the resistance of the n-channel between drain and source.
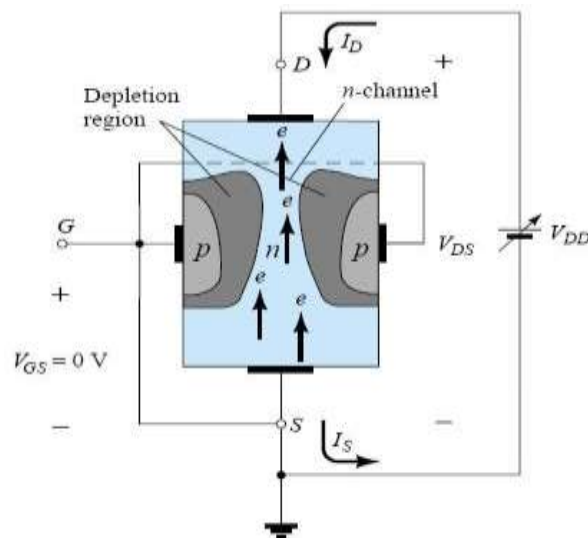
Fig 1.3 JFET in the $V_{GS} = 0$ V and $V_{DS} > 0$ V

As the voltage V_{DS} is increased from 0 to a few volts, the current will increase as determined by Ohm's law and the plot of I_D versus V_{DS} will appear as shown in Fig. 1.4. The relative straightness of the plot reveals that for the region of low values of V_{DS}, the resistance is essentially constant. As V_{DS} increases and approaches a level referred to as V_P in Fig. 1.4, the depletion regions of Fig. 1.3 will widen, causing a noticeable reduction in the channel width. The reduced path of conduction causes the resistance to increase and the curve in the graph of Fig. 1.4 to occur. The more horizontal the curve, the higher the resistance, suggesting that the resistance is approaching "infinite" ohms in the horizontal region.
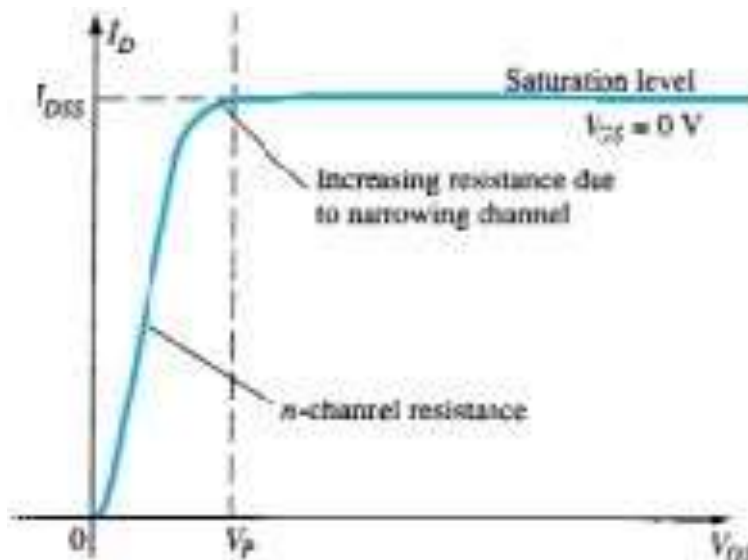

Fig 1.4 I_D versus V_{DS} for V_{GS}=0 V

If V_{DS} is increased to a level where it appears that the two depletion regions would "touch" as shown in Fig. 1.5, a condition referred to as *pinch-off* will result. The level of V_{DS} that establishes this condition is referred to as the *pinch-off voltage* and is denoted by V_P as shown in Fig. 1.4. In actuality, the term *pinch-off* suggests the current I_D is pinched off and drops to 0 A. As shown in Fig. 1.4, I_D maintains a saturation level defined as I_{DSS}. In reality a very small channel still exists, with a current of very high density. The fact that I_D does not drop off at pinch-off and maintains the saturation level indicated in Fig. 1.4 is verified by the following fact: The absence of a drain current would remove the possibility of different potential levels through the *n*-channel material to establish the varying levels of reverse bias along the *p-n* junction. The result would be a loss of the depletion region distribution that caused pinch-off in the first place.
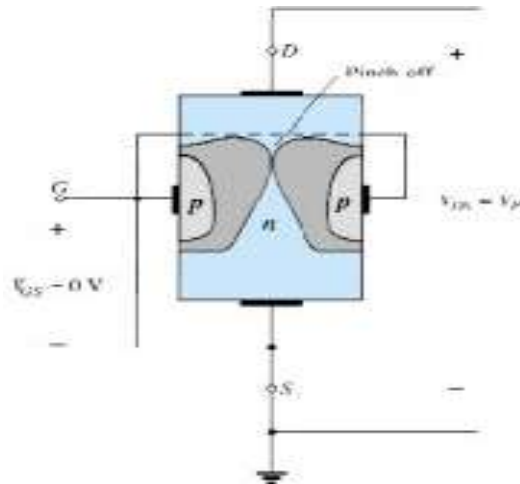
Fig 1.5 Pinch-off ($V_{GS} = 0$ V, $V_{DS} = V_P$)

As V_{DS} is increased beyond V_P, the region of close encounter between the two depletion regions will increase in length along the channel, but the level of I_D remains essentially the same. In essence, therefore, once $V_{DS} = V_P$ the JFET has the characteristics of a current source. As shown in Fig. 5.8, the current is fixed at $I_D = I_{DSS}$, but the voltage V_{DS} (for levels $> V_P$) is determined by the applied load.

I_{DSS} is the maximum drain current for a JFET and is defined by the conditions $V_{GS} = 0$ V and $V_{DS} > |V_P|$.
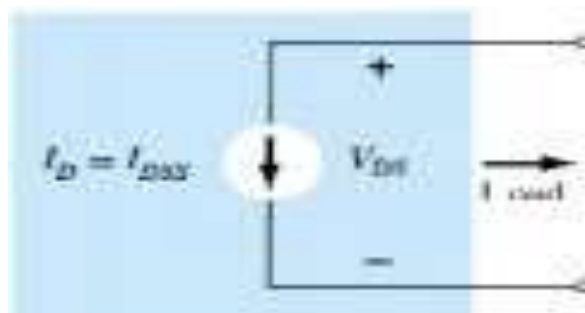

Fig 1.6 Current source equivalent for $V_{GS} = 0$ V, $V_{DS} > V_P$

VGS = 0 V

The voltage from gate to source, denoted V_{GS}, is the controlling voltage of the JFET. Just as various curves for I_C versus V_{CE} were established for different levels of I_B for the BJT transistor, curves of I_D versus V_{DS} for various levels of V_{GS} can be developed for the JFET. For the n-channel device the controlling voltage V_{GS} is made more and more negative from its $V_{GS} = 0$ V level. In other words, the gate terminal will be set at lower and lower potential levels as compared to the source.

In Fig. 1.7 a negative voltage of -1 V has been applied between the gate and source terminals for a low level of V_{DS}. The effect of the applied negative-bias

V_{GS} is to establish depletion regions similar to those obtained with $V_{GS} = 0$ V but at lower levels of V_{DS}. Therefore, the result of applying a negative bias to the gate is to reach the saturation level at a lower level of V_{DS} as shown in Fig. 1.8 for $V_{GS} = -1$ V.
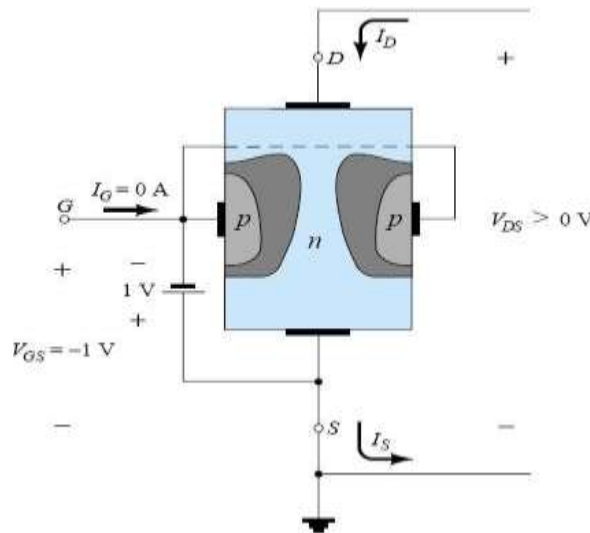

Fig 1.7 Application of a negative voltage to the gate of a JFET

The resulting saturation level for I_D has been reduced and in fact will continue to decrease as V_{GS} is made more and more negative. Note also on Fig. 1.8 how the pinch-off voltage continues to drop in a parabolic manner as V_{GS} becomes more and more negative. Eventually, V_{GS} when $V_{GS} = -V_P$ will be sufficiently negative to establish a saturation level that is essentially 0 mA, and for all practical purposes the device has been "turned off."

In summary:

The level of V_{GS} that results in $I_D = 0$ mA is defined by $V_{GS} = V_P$, with V_P being a negative voltage for n-channel devices and a positive voltage for p-channel JFETs.
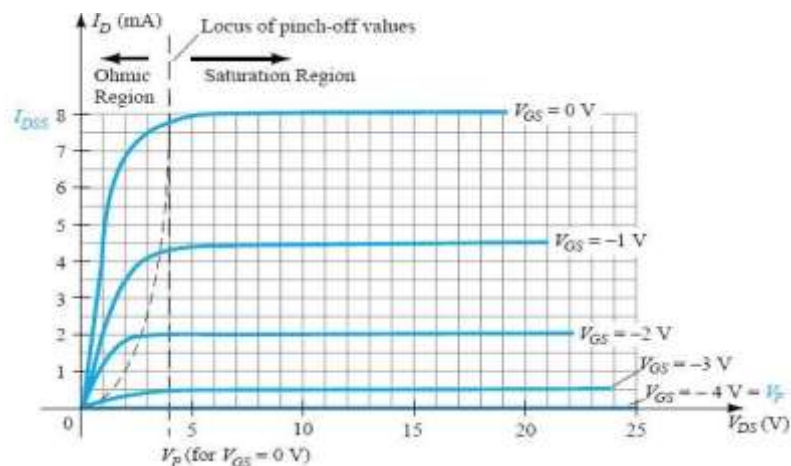

Fig 1.8 n-Channel JFET characteristics with $I_{DSS} = 8$ mA and $V_P = 4$ V

The region to the right of the pinch-off locus of Fig. 1.8 is the region typically employed in linear amplifiers (amplifiers with minimum distortion of the applied signal) and is commonly referred to as the *constant-current, saturation,* or *linear amplification region.*

Voltage-Controlled Resistor

The region to the left of the pinch-off locus of Fig. 1.8 is referred to as the *ohmic* or *voltage-controlled resistance region.* In this region the JFET can actually be employed as a variable resistor (possibly for an automatic gain control system) whose resistance is controlled by the applied gate-to-source voltage. Note in Fig. 1.8 that the slope of each curve and therefore the resistance of the device between drain and source for $V_{DS} = V_P$ is a function of the applied voltage V_{GS}. As V_{GS} becomes more and more negative, the slope of each curve becomes more and more horizontal, corresponding with an increasing resistance level.

$$\mathbf{r_d = r_0 / [1- (V_{GS}/V_P)^2]} \text{ ----------------------------- (5.1)}$$

where r_o is the resistance with $V_{GS} = 0$ V and r_d the resistance at a particular level of V_{GS}.

P-Channel Devices

The *p*-channel JFET is constructed in exactly the same manner as the *n*-channel device of Fig. 1.2, but with a reversal of the *p*- and *n*- type materials as shown in Fig. 1.9.
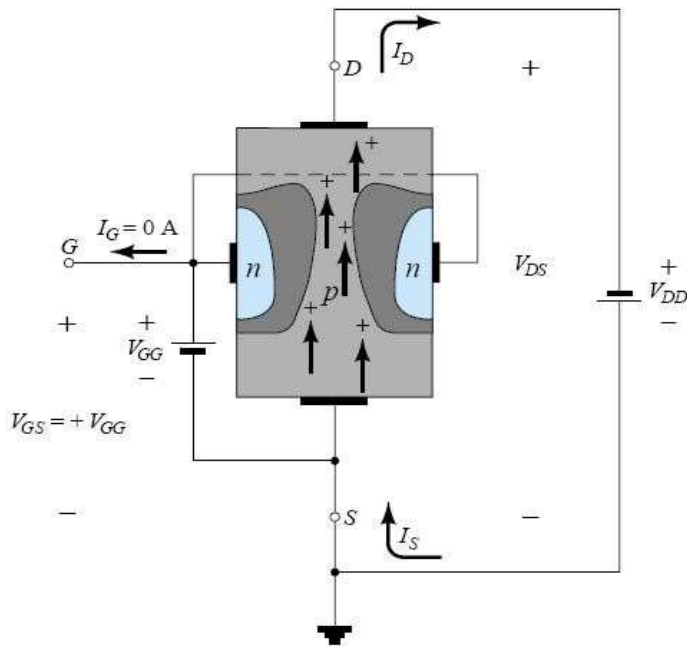

Fig 1.9 *p*-Channel JFET

The defined current directions are reversed, as are the actual polarities for the voltages V_{GS} and V_{DS}. For the *p*-channel device, the channel will be constricted by increasing positive voltages from gate to source and the double-subscript notation for V_{DS} will result in negative voltages for V_{DS} on the characteristics of Fig. 1.10, which has an I_{DSS} of 6 mA and a pinch-off voltage of $V_{GS} = +6$ V. Do not let the minus signs for V_{DS} confuse you. They simply indicate that the source is at a higher potential than the drain.
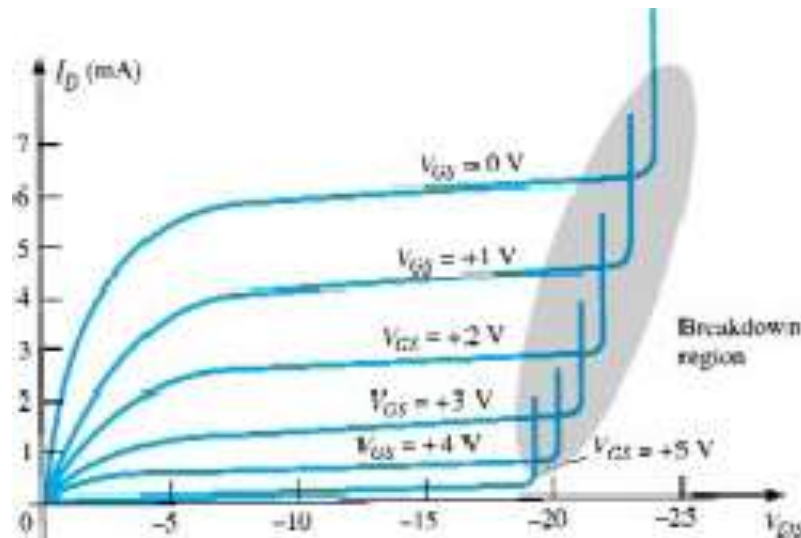

Fig 1.10 *p*-Channel JFET characteristics with $I_{DSS} = 6$ mA and $V_P = +6$ V

Note at high levels of V_{DS} that the curves suddenly rise to levels that seem unbounded. The vertical rise is an indication that breakdown has occurred and the current through the channel (in the same direction as normally encountered) is now limited solely by the external circuit. Although not appearing in Fig. 1.8 for the *n*-channel device, they do occur for the *n*-channel device if sufficient voltage is applied. This region can be avoided if the level of $V_{DS\max}$ is noted on the specification sheet and the design is such that the actual level of V_{DS} is less than this value for *all* values of V_{GS}.

Symbols

The graphic symbols for the *n*-channel and *p*-channel JFETs are provided in Fig. 1.11. Note that the arrow is pointing in for the *n*-channel device of Fig. 1.11(a) to represent the direction in which I_G would flow if the *p-n* junction were forward-biased. For the *p*-channel device (Fig. 1.11(b)) the only difference in the symbol is the direction of the arrow.
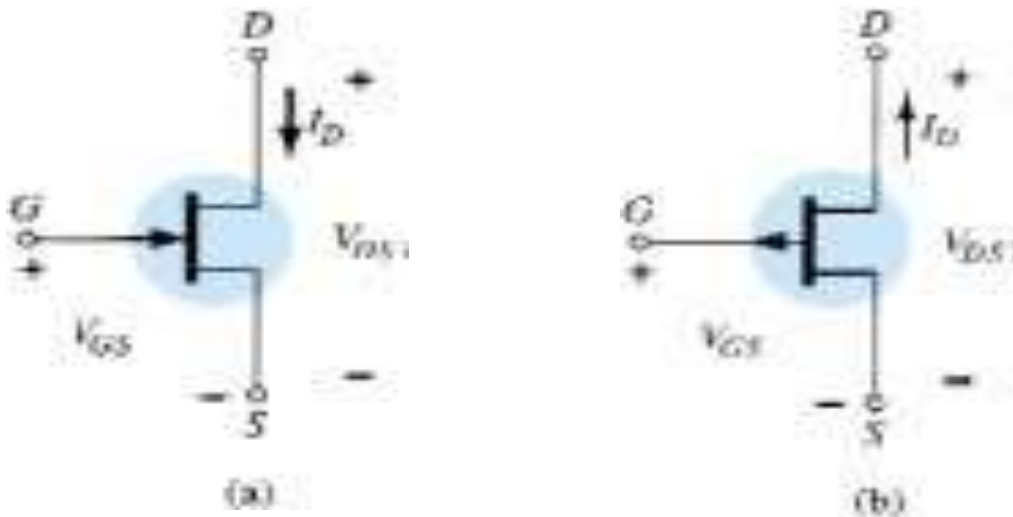
Fig 1.11 JFET symbols: (a) *n*-channel; (b) *p*-channel

Summary

- *The maximum current is defined as I_{DSS} and occurs when $V_{GS} = 0\ V$ and VDS $\geq |VP|$ as shown in Fig. 1.12(a).*
- *For gate-to-source voltages V_{GS} less than (more negative than) the pinch-off level, the drain current is 0 A ($I_D = 0\ A$) as appearing in Fig. 1.12(b).*
- *For all levels of V_{GS} between 0 V and the pinch-off level, the current I_D will range between I_{DSS} and 0 A, respectively, as reviewed by Fig. 1.12(c).*
- *For p-channel JFETs a similar list can be developed.*
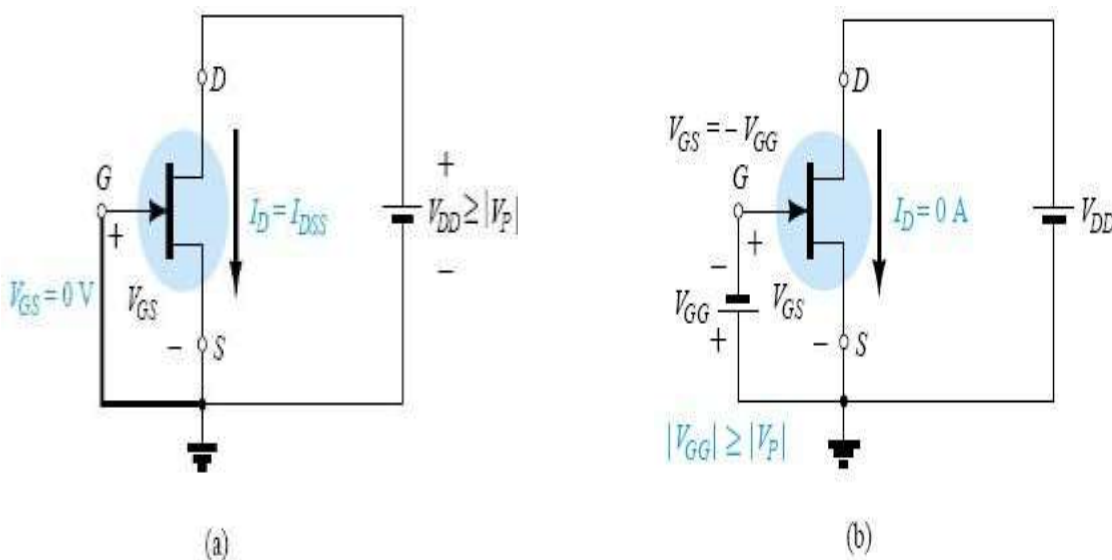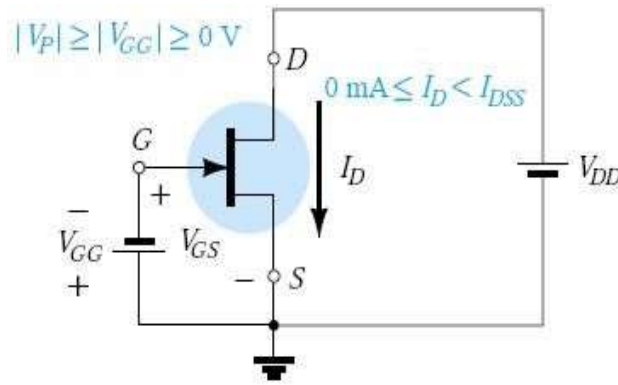
(c)

Fig 1.12 (a) V_{GS} =0 V, $I_D = I_{DSS}$; (b) cutoff (I_D = 0 A) V_{GS} less than the pinch-off level; (c) I_D exists between 0 A and I_{DSS} for V_{GS} less than or equal to 0 V and greater than the pinch-off level.

1.3   TRANSFER CHARACTERISTICS

For the BJT transistor the output current I_C and input controlling current I_B were related by beta, which was considered constant for the analysis to be performed. In equation form,

$$I_C = f(I_B) = \beta I_B \text{----------------- (1.2)}$$

In Eq. (1.2) a linear relationship exists between I_C and I_B. Double the level of I_B and I_C will increase by a factor of two also.

Unfortunately, this linear relationship does not exist between the output and input quantities of a JFET. The relationship between I_D and V_{GS} is defined by *Shockley's equation:*

$$\mathbf{I_D = I_{DSS}(1\text{- }V_{GS}/V_P)^2} \text{----------- (1.3)}$$

The squared term of the equation will result in a nonlinear relationship between I_D and V_{GS}, producing a curve that grows exponentially with decreasing magnitudes of V_{GS}.

The graphical approach, however, will require a plot of Eq. (1.3) to represent the device and a plot of the network equation relating the same variables. The solution is defined by the point of intersection of the two curves. It is important to keep in mind when applying the graphical approach that the device characteristics will be *unaffected* by the network in which the device is employed. The network equation may change along with the intersection between the two curves, but the transfer curve defined by Eq. (1.3) is unaffected.

In general, therefore:
The transfer characteristics defined by Shockley's equation are unaffected by the network in which the device is employed.

The transfer curve can be obtained using Shockley's equation or from the output characteristics of Fig. 1.8. In Fig. 1.13 two graphs are provided, with the vertical scaling in milli amperes for each graph. One is a plot of I_D versus V_{DS}, while the other is I_D versus V_{GS}. Using the drain characteristics on the right of the "y" axis, a horizontal line can be drawn from the saturation region of the curve denoted $V_{GS} = 0$ V to the I_D axis. The resulting current level for both graphs is I_{DSS}. The point of intersection on the I_D versus V_{GS} curve will be as shown since the vertical axis is defined as $V_{GS} = 0$ V.
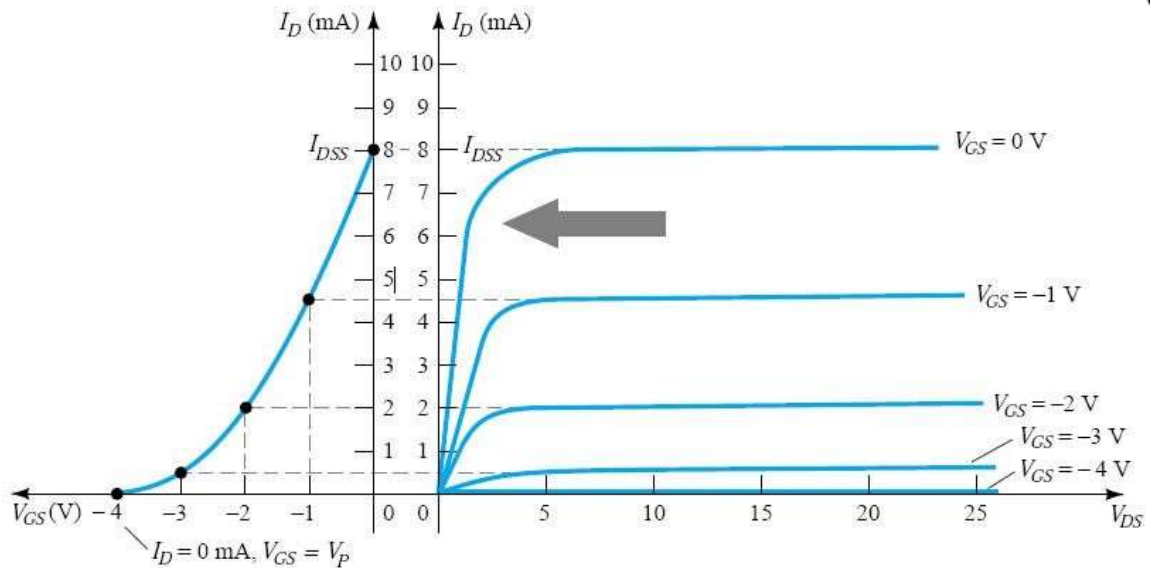

Fig 1.13 Obtaining the transfer curve from the drain characteristics

In review:
When $V_{GS} = 0$ V, $I_D = I_{DSS}$.

When $V_{GS} = V_P = -4$ V, the drain current is zero milli amperes, defining another point on the transfer curve. That is:
When $V_{GS} = V_P$, $I_D = 0$ mA.

The drain characteristics relate one output (or drain) quantity to another output (or drain) quantity—both axes are defined by variables in the same region of the device characteristics. The transfer characteristics are a plot of an output (or drain) current versus an input-controlling quantity. There is therefore a direct "transfer" from input to output variables when employing the curve to the left of Fig. 1.13. If the relationship were linear, the plot of I_D versus V_{GS} would result in a straight line between I_{DSS} and V_P. However, a parabolic curve will result because the vertical spacing between steps of V_{GS} on the drain characteristics of Fig. 1.13 decreases noticeably as V_{GS} becomes more and more negative.
Compare the spacing between $V_{GS} = 0$ V and $V_{GS} = -1$ V to that between $V_{GS} = -3$ V and pinch-off. The change in V_{GS} is the same, but the resulting change in I_D is quite different.

Applying Shockley's Equation

The transfer curve of Fig. 1.13 can also be obtained directly from Shockley's equation (1.3) given simply the values of I_{DSS} and V_P. The levels of I_{DSS} and V_P define the limits of the curve on both axes and leave only the necessity of finding a few intermediate plot points.
Substituting $V_{GS} = 0$ V in equation 1.3 gives,

$$\mathbf{I_D = I_{DSS}|_{VGS = 0v}} \text{-------------(1.4)}$$

Substituting $V_{GS} = V_P$ yields,

$$\mathbf{I_D = 0V|_{VGS = VP}} \text{-------------(1.5)}$$

For the drain characteristics of Fig. 1.13, if we substitute $V_{GS} = -1$ V,

$$I_D = 4.5\text{mA}$$

as shown in Fig. 1.13. Note the care taken with the negative signs for V_{GS} and V_P in the calculations above. The loss of one sign would result in a totally erroneous result.

It should be obvious from the above that given I_{DSS} and V_P (as is normally provided on specification sheets) the level of I_D can be found for any level of V_{GS}. Conversely, an equation for the resulting level of V_{GS} for a given level of I_D

$$\mathbf{V_{GS} = V_P \left(1 - \sqrt{\frac{ID}{IDSS}}\right)} \text{---------------------(1.6)}$$

Shorthand Method

$$I_D = I_{DSS}|_{VGS = VP/2} \text{--------------------- (1.7)}$$

$$V_{GS} = 0.3V_P|_{ID = IDSS/2} \text{----------------- (1.8)}$$

TABLE 5.1 V_{GS} versus I_D Using Shockley's Equation

V_{GS}	I_D
0	I_{DSS}
0.3 V_P	$I_{DSS}/2$
0.5 V_P	$I_{DSS}/4$
V_P	0 mA

1.4   <u>IMPORTANT RELATIONSHIPS</u>
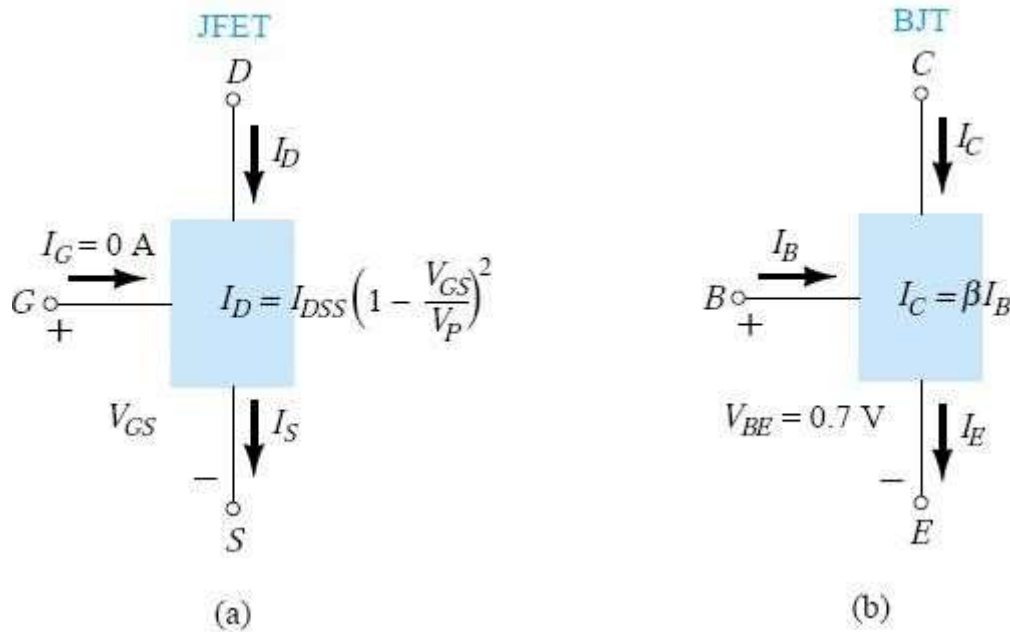
Fig 1.14 (a) JFET versus (b) BJT

A clear understanding of the impact of each of the equations above is sufficient background to approach the most complex of dc configurations. Recall that V_{BE} = 0.7 V was often the key to initiating an analysis of a BJT configuration. Similarly, the condition $I_G = 0$ A is often the starting point for the analysis of a JFET configuration.

For the BJT configuration, I_B is normally the first parameter to be determined.

For the JFET, it is normally V_{GS}.

1.5 DEPLETION-TYPE MOSFET

There are two types of FETs: JFETs and MOSFETs. MOSFETs are further broken down into *depletion type* and *enhancement type.* The terms *depletion* and *enhancement* define their basic mode of operation, while the label MOSFET stands for *m*etal-*o*xide-*s*emiconductor-*f*ield-*e*ffect *t*ransistor. the depletion-type MOSFET, which happens to have characteristics similar to those of a JFET between cut-off and saturation at I_{DSS} but then has the added feature of characteristics that extend into the region of opposite polarity for V_{GS}.

Basic Construction

The basic construction of the *n*-channel depletion-type MOSFET is provided in Fig. 1.15. A slab of *p*-type material is formed from a silicon base and is referred to as the *substrate.* It is the foundation upon which the device will be constructed. In some cases the substrate is internally connected to the source terminal. However, many discrete devices provide an additional terminal labelled *SS*, resulting in a four-terminal device, such as that appearing in Fig. 1.15. The source and drain terminals are connected through metallic contacts to *n*-doped regions linked by an *n*-channel as shown in the figure. The gate is also connected to a metal contact surface but remains insulated from the *n*-channel by a very thin silicon dioxide (SiO_2) layer. SiO_2 is a particular type of insulator referred to as a *dielectric* that sets up opposing electric fields within the dielectric when exposed to an externally applied field.
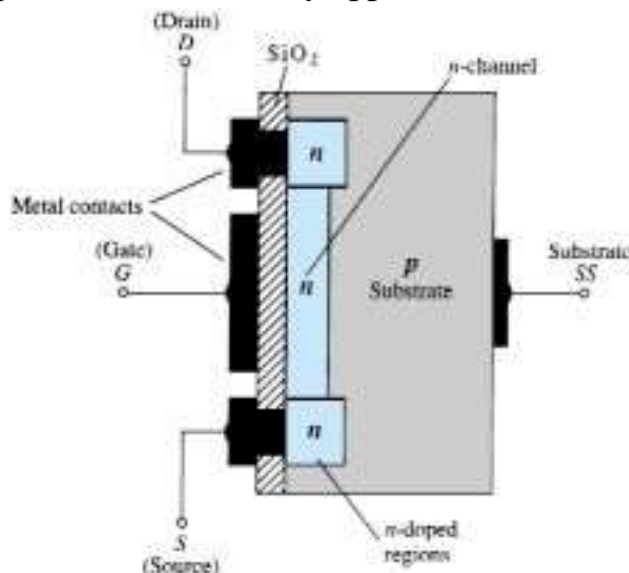

Fig 1.15 *n*-Channel depletion-type MOSFET

The fact that the SiO_2 layer is an insulating layer reveals the following fact:
There is no direct electrical connection between the gate terminal and the channel of a MOSFET.

In addition:

It is the insulating layer of SiO₂ in the MOSFET construction that accounts
for the very desirable high input impedance of the device.

In fact, the input resistance of a MOSFET is often that of the typical JFET, even though the input impedance of most JFETs is sufficiently high for most applications. The very high input impedance continues to fully support the fact that the gate current (I_G) is essentially zero amperes for dc-biased configurations. The reason for the label metal-oxide-semiconductor FET is now fairly obvious: *metal* for the drain, source, and gate connections to the proper surface—in particular, the gate terminal and the control to be offered by the surface area of the contact, the *oxide* for the silicon dioxide insulating layer, and the *semiconductor* for the basic structure on which the *n*- and *p*-type regions are diffused. The insulating layer between the gate and channel has resulted in another name for the device: *insulated gate FET* or *IGFET,* although this label is used less and less in current literature.

Basic Operation and Characteristics

In Fig. 1.16 the gate-to-source voltage is set to zero volts by the direct connection from one terminal to the other, and a voltage V_{DS} is applied across the drain-to-source terminals. The result is an attraction for the positive potential at the drain by the *free* electrons of the *n*-channel and a current similar to that established through the channel of the JFET. In fact, the resulting current with $VGS = 0$ V continues to be labelled I_{DSS}, as shown in Fig. 1.17.
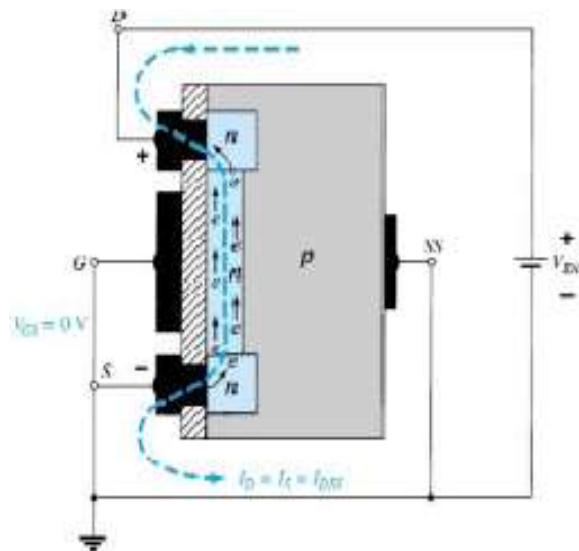

Fig 1.16 *n*-Channel depletion-type MOSFET with $VGS = 0$ V
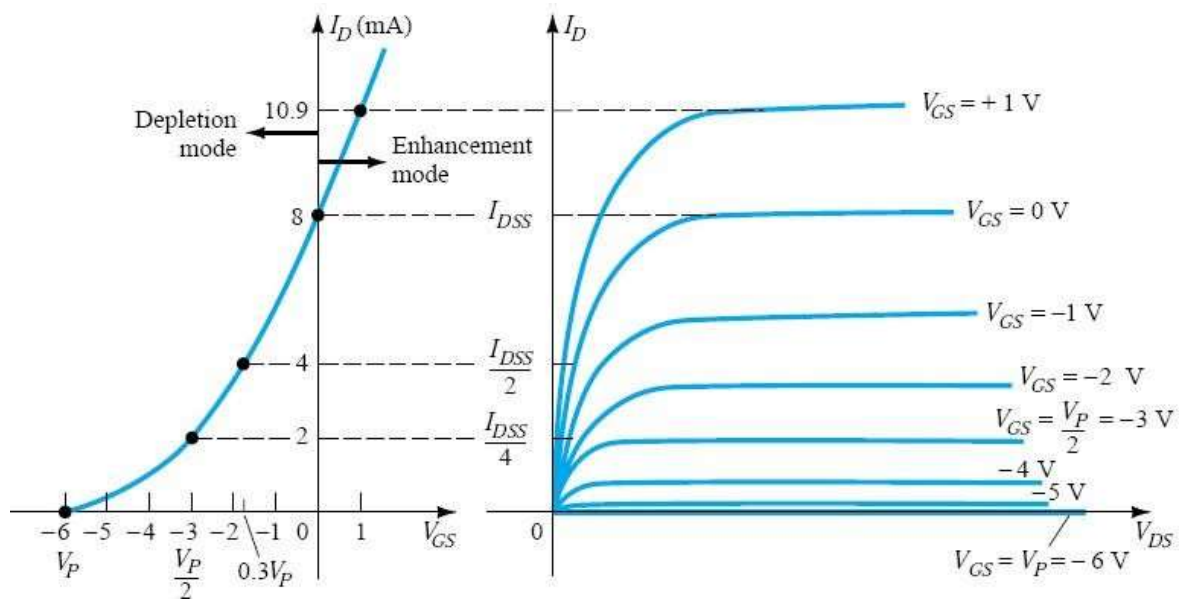and an applied voltage V_{DD}

Fig 1.17 Drain and transfer characteristics for an *n*-channel depletion-type MOSFET

The region of positive gate voltages on the drain or transfer characteristics is often referred to as the *enhancement region,* with the region between cut-off and the saturation level of I_{DSS} referred to as the *depletion region.* Shockley's equation is applicable for the depletion-type MOSFET characteristics in both the depletion and enhancement regions. For both regions, it is simply necessary that the proper sign be included with V_{GS} in the equation and the sign be carefully monitored in the mathematical operations.

p-Channel Depletion-Type MOSFET

The construction of a *p*-channel depletion-type MOSFET is exactly the reverse of that appearing in Fig. 1.15. There is an *n*-type substrate and a *p*-type channel, as shown in Fig. 1.18(a). The terminals remain as identified, but all the voltage polarities and the current directions are reversed, as shown in the same figure. The drain characteristics would appear exactly as in Fig. 1.16 but with V_{DS} having negative values I_D having positive values as indicated (since the defined direction is now reversed), and V_{GS} having the opposite polarities as shown in Fig. 1.18(c). The reversal in V_{GS} will result in a mirror image (about the I_D axis) for the transfer characteristics as shown in Fig. 1.18(b). In other words, the drain current will increase from cut-off at $V_{GS} = V_P$ in the positive V_{GS} region to I_{DSS} and then continue to increase for increasingly negative values of V_{GS}. Shockley's equation is still applicable and requires simply placing the correct sign for both V_{GS} and V_P in the equation.
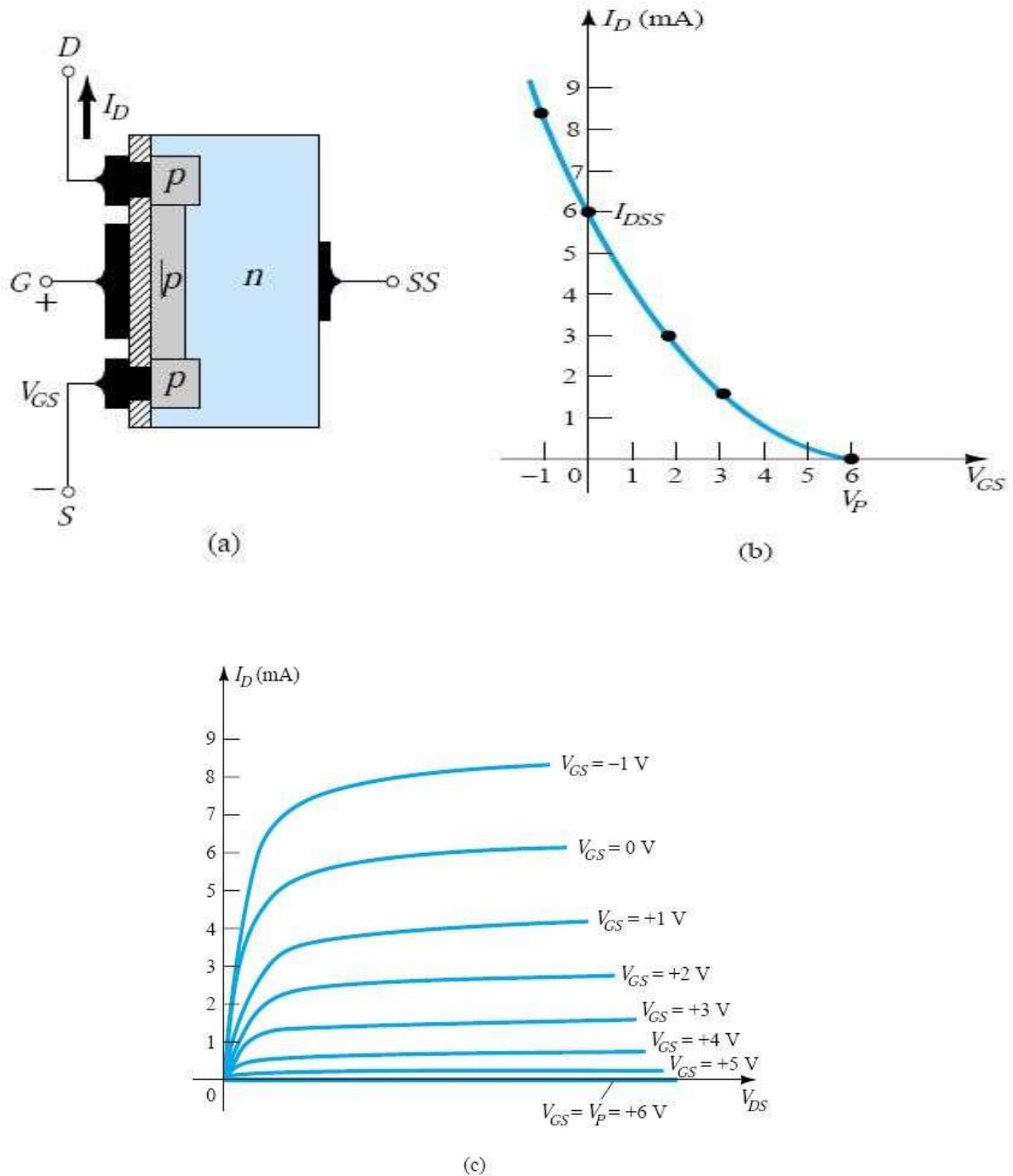
Fig 1.18 *p*-Channel depletion-type MOSFET with I_{DSS} = 6 mA and V_P = -6 V

Symbols

The graphic symbols for an *n*- and *p*-channel depletion-type MOSFET are provided in Fig. 1.19. The lack of a direct connection (due to the gate insulation) between the gate and channel is represented by a space between the gate and the other terminals of the symbol. The vertical line representing the channel is connected between the drain and source and is "supported" by the substrate. Two symbols are provided for each type of channel to reflect the fact that in some cases the substrate is externally available while in others it is not.
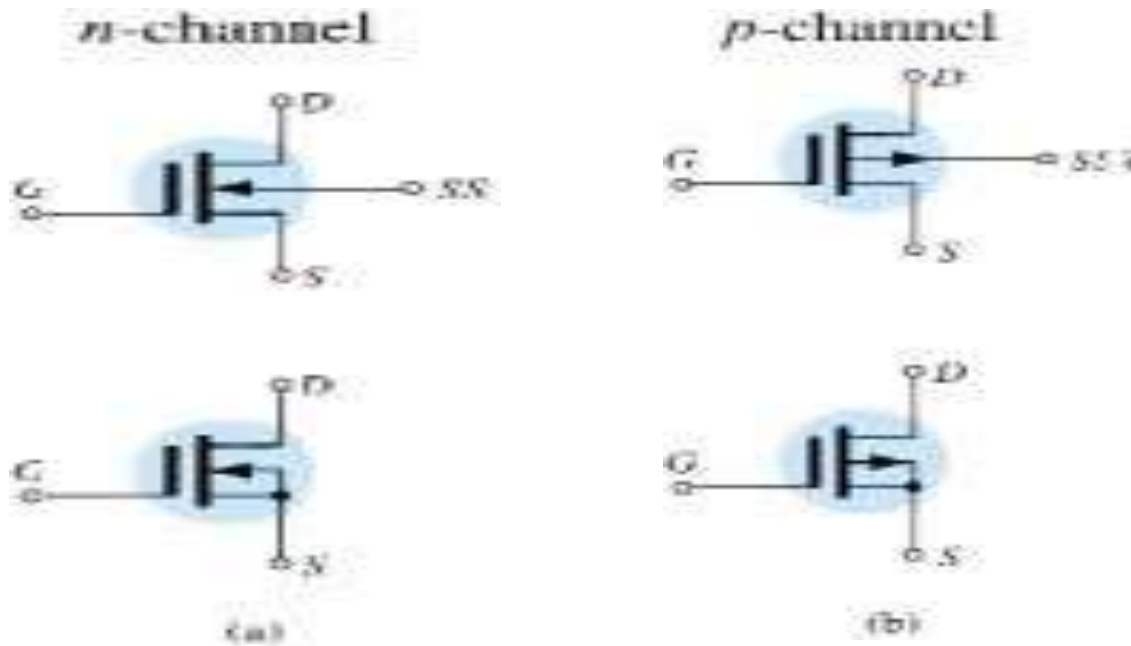
Fig 1.19 Graphic symbols for (a) *n*-channel depletion-type MOSFETs
and (b) *p*- channel depletion-type MOSFETs

1.6 ENHANCEMENT-TYPE MOSFET

Although there are some similarities in construction and mode of operation between depletion-type and enhancement-type MOSFETs, the characteristics of the enhancement-type MOSFET are quite different from anything obtained thus far. The transfer curve is not defined by Shockley's equation, and the drain current is now cut off until the gate-to-source voltage reaches a specific magnitude. In particular, current control in an *n*-channel device is now effected by a positive gate-to-source voltage rather than the range of negative voltages encountered for *n*-channel JFETs and *n*-channel depletion-type MOSFETs.

Basic Construction

The basic construction of the *n*-channel enhancement-type MOSFET is provided in Fig. 1.20. A slab of *p*-type material is formed from a silicon base and is again referred to as the substrate. As with the depletion-type MOSFET, the substrate is sometimes internally connected to the source terminal, while in other cases a fourth lead is made available for external control of its potential level. The source and drain terminals are again connected through metallic contacts to *n*-doped regions, but note in Fig. 1.20 the absence of a channel between the two *n*-doped regions. This is the primary difference between the construction of depletion-type and enhancement-type MOSFETs—the absence of a channel as a constructed component of the device. The SiO_2 layer is still present to isolate the gate metallic platform from the region between the drain and source, but now it is simply separated from a section of the *p*-type material.

In summary, therefore, the *construction of an enhancement-type MOSFET is quite similar to that of the depletion-type MOSFET, except for the absence of a channel between the drain and source terminals*.
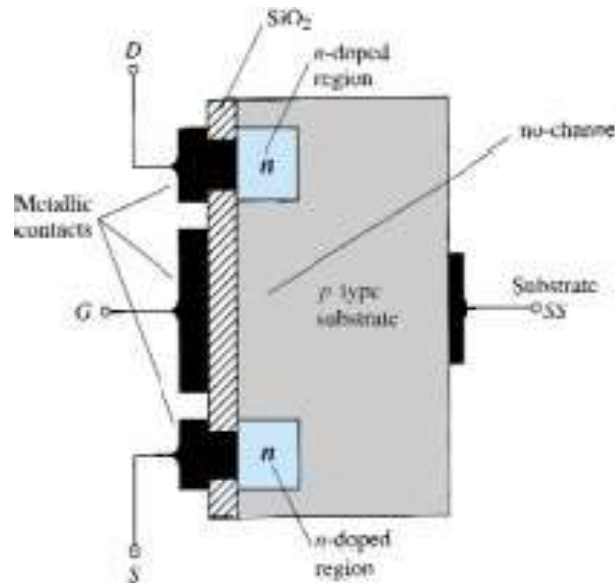

Fig 1.20 *n*-Channel enhancement-type MOSFET

Basic Operation and Characteristics

If V_{GS} is set at 0 V and a voltage applied between the drain and source of the device of Fig. 1.20, the absence of an *n*-channel (with its generous number of free carriers) will result in a current of effectively zero amperes—quite different from the depletion-type MOSFET and JFET where $I_D = I_{DSS}$. It is not sufficient to have a large accumulation of carriers (electrons) at the drain and source (due to the *n*-doped regions) if a path fails to exist between the two. With V_{DS} some positive voltage, V_{GS} at 0 V, and terminal *SS* directly connected to the source, there are in fact two reverse-biased *p-n* junctions between the *n*-doped regions and the *p*-substrate to oppose any significant flow between drain and source.

In Fig. 1.21 both V_{DS} and V_{GS} have been set at some positive voltage greater than 0 V, establishing the drain and gate at a positive potential with respect to the source. The positive potential at the gate will pressure the holes (since like charges repel) in the *p*-substrate along the edge of the SiO_2 layer to leave the area and enter deeper regions of the *p*-substrate, as shown in the figure. The result is a depletion region near the SiO_2 insulating layer void of holes. However, the electrons in the *p*-substrate (the minority carriers of the material) will be attracted to the positive gate and accumulate in the region near the surface of the SiO_2 layer. The SiO_2 layer and its insulating qualities will prevent the negative carriers from being absorbed at the gate terminal. As V_{GS} increases in magnitude, the concentration of electrons near the SiO_2 surface increases until eventually the induced *n*-type region can support a measurable flow between drain and source. The level of V_{GS} that results in the significant

increase in drain current is called the *threshold voltage* and is given the symbol V_T. On specification sheets it is referred to as $V_{GS(Th)}$, although V_T is less unwieldy and will be used in the analysis to follow. Since the channel is nonexistent with $V_{GS} = 0$ V and "enhanced" by the application of a positive gate-to-source voltage, this type of MOSFET is called an *enhancement-type MOSFET*. Both depletion- and enhancement-type MOSFETs have enhancement-type regions, but the label was applied to the latter since it is its only mode of operation.
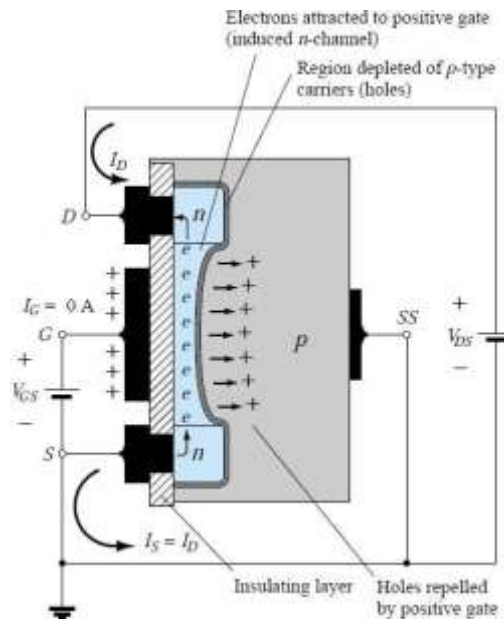
Fig 1.21 Channel formation in the *n*-channel enhancement-type MOSFET

As V_{GS} is increased beyond the threshold level, the density of free carriers in the induced channel will increase, resulting in an increased level of drain current. However, if we hold V_{GS} constant and increase the level of V_{DS}, the drain current will eventually reach a saturation level as occurred for the JFET and depletion-type MOSFET. The levelling off of I_D is due to a pinching-off process depicted by the narrower channel at the drain end of the induced channel as shown in Fig. 1.22. Applying Kirchhoff's voltage law to the terminal voltages of the MOSFET of Fig. 1.23, we find that
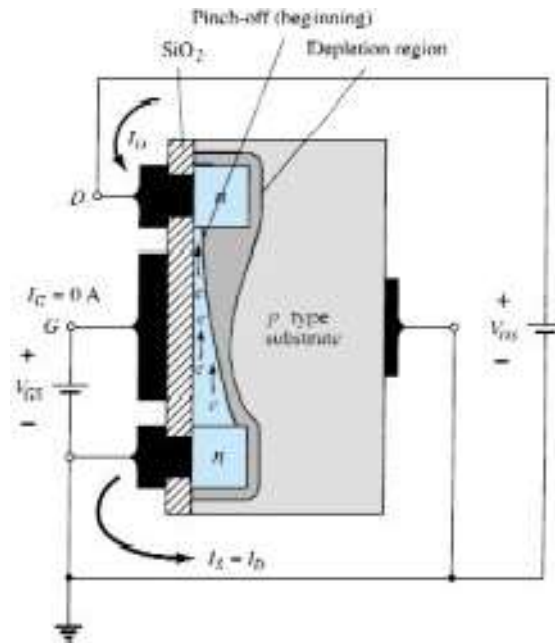
$$V_{DG} = V_{DS} - V_{GS} \text{ ----------------------(1.9)}$$

Fig 1.22 Change in channel and depletion region with increasing level of V_{DS} for a fixed value of V_{GS}

If V_{GS} is held fixed at some value such as 8 V and V_{DS} is increased from 2 to 5 V, the voltage V_{DG} [by Eq. (1.9)] will drop from -6 to -3 V and the gate will become less and less positive with respect to the drain. This reduction in gate-to-drain voltage will in turn reduce the attractive forces for free carriers (electrons) in this region of the induced channel, causing a reduction in the effective channel width. Eventually, the channel will be reduced to the point of pinch-off and a saturation condition will be established as described earlier for the JFET and depletion-type MOSFET.

In other words, any further increase in V_{DS} at the fixed value of V_{GS} will not affect the saturation level of I_D until breakdown conditions are encountered. The drain characteristics of Fig. 1.23 reveal that for the device of Fig. 1.22 with $V_{GS} = 8$ V, saturation occurred at a level of $V_{DS} = 6$ V. In fact, the saturation level for V_{DS} is related to the level of applied V_{GS} by

$$\textbf{V}_{\textbf{DSsat}} = \textbf{V}_{\textbf{GS}} \textbf{ - } \textbf{V}_{\textbf{T}} \text{ ---------------------- (1.10)}$$

Therefore, for a fixed value of V_T, then the higher the level of V_{GS}, the more the saturation level for V_{DS}, as shown in Fig. 1.22 by the locus of saturation levels. For the characteristics of Fig. 1.22 the level of V_T is 2 V, as revealed by the fact that the drain current has dropped to 0 mA.

In general, therefore:
For values of V_{GS} less than the threshold level, the drain current of an enhancement-type MOSFET is 0 mA.

Fig 1.23 clearly reveals that as the level of V_{GS} increased from V_T to 8 V, the resulting saturation level for I_D also increased from a level of 0 to 10 mA. In addition, it is quite noticeable that the spacing between the levels of V_{GS} increased as the magnitude of V_{GS} increased, resulting in ever-increasing increments in drain current.

For levels of $V_{GS} > V_T$, the drain current is related to the applied gate-to-source voltage by the following nonlinear relationship:

$$\mathbf{I_D = k(V_{GS} - V_T)^2} \text{ -------------------------------- (1.11)}$$

Again, it is the squared term that results in the nonlinear (curved) relationship between I_D and V_{GS}. The k term is a constant that is a function of the construction of the device. The value of k can be determined from the following equation [derived from Eq. (1.11)] where I_D(on) and V_{GS}(on) are the values for each at a particular point on the characteristics of the device.

$$\mathbf{k = I_D(on)/[V_{GS}(on) - V_T]^2} \text{ -------------------------(1.12)}$$
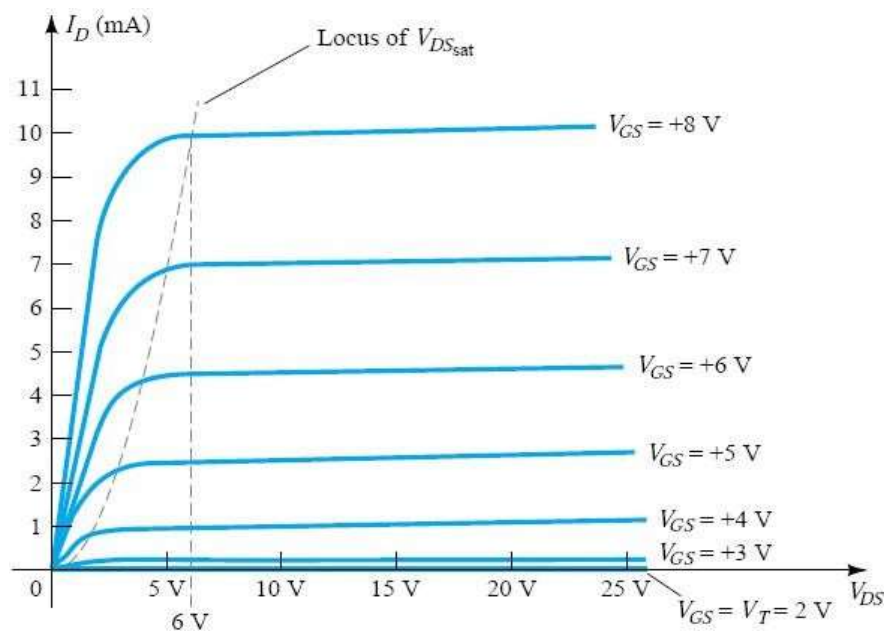
Fig 1.23 Drain characteristics of an *n*-channel enhancement-type MOSFET with $V_T = 2$ V and $k = 0.278 \times 10^3$ A/V^2
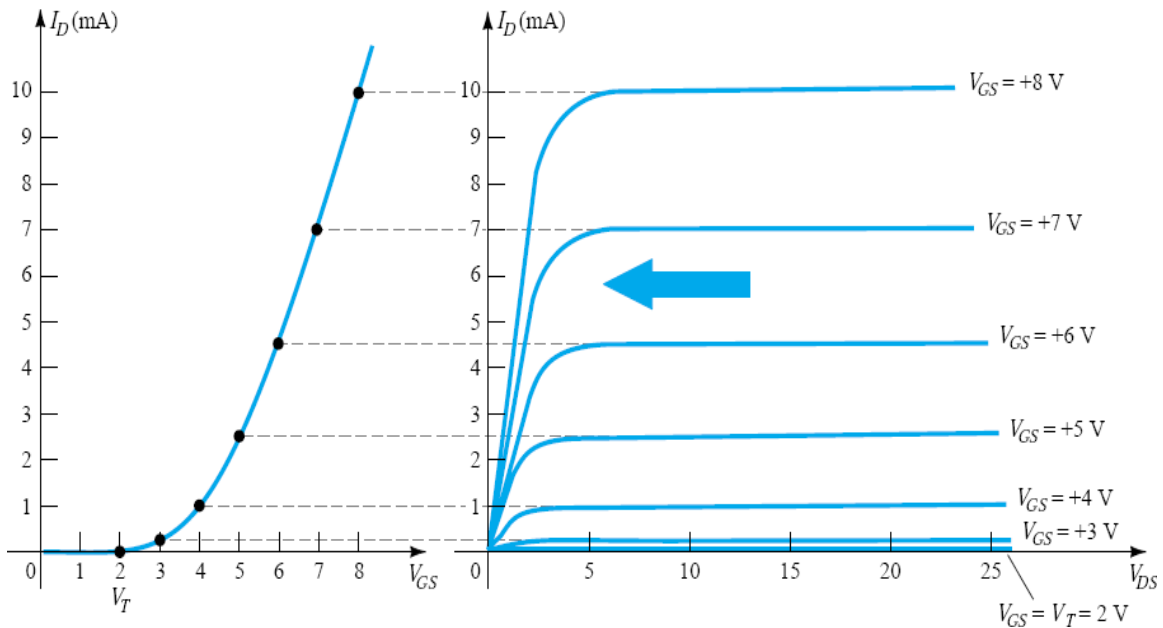
Fig 1.24 Transfer characteristics for an *n*-channel enhancement-type MOSFET
from the drain characteristics

p-Channel Enhancement-Type MOSFETs

The construction of a *p*-channel enhancement-type MOSFET is exactly the reverse of that appearing in Fig. 1.20, as shown in Fig. 1.25(a). There is now an *n*-type substrate and *p*-doped regions under the drain and source connections. The terminals remain as identified, but all the voltage polarities and the current directions are reversed. The drain characteristics will appear as shown in Fig. 1.25(c), with increasing levels of current resulting from increasingly negative values of V_{GS}. The transfer characteristics will be the mirror image (about the I_D axis) of the transfer curve of Fig. 1.24, with I_D increasing with increasingly negative values of V_{GS} beyond V_T, as shown in Fig. 1.25(b). Equations (1.9) through (1.12) are equally applicable to *p*-channel devices.
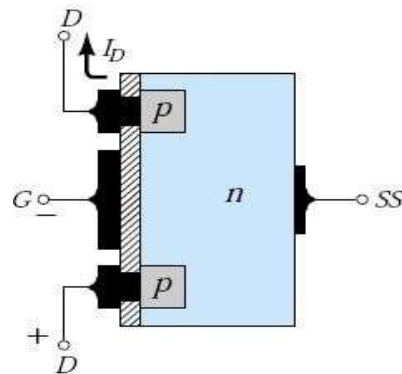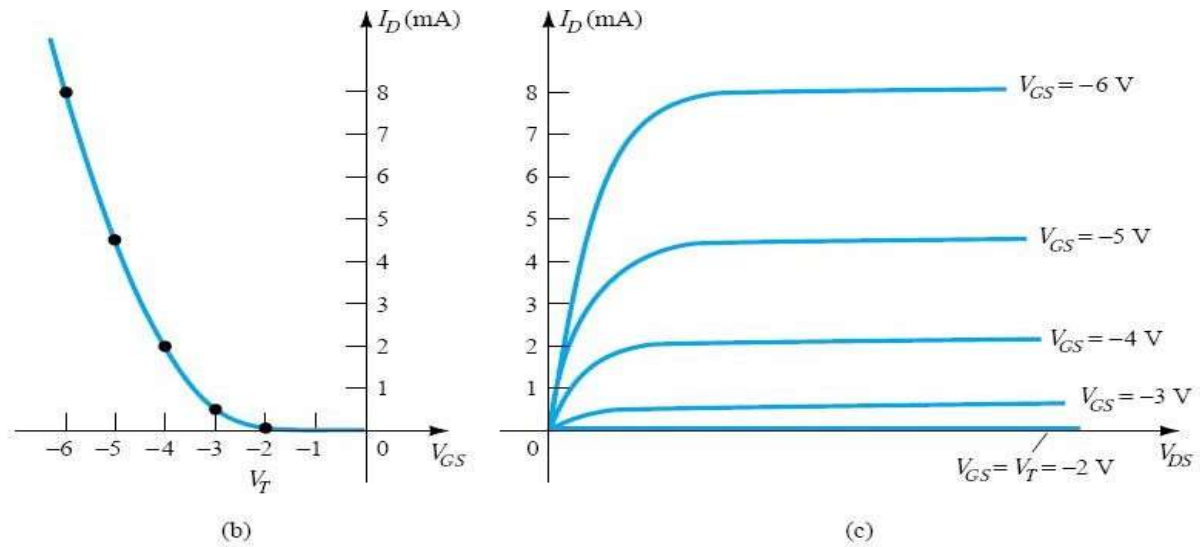

(a)

Fig 1.25 *p*-Channel enhancement-type MOSFET
with $V_T = 2$ V and $k = 0.5 \times 10^3$ A/V^2

Symbols

The graphic symbols for the *n*- and *p*-channel enhancement-type MOSFETs are provided as Fig. 1.26. Again note how the symbols try to reflect the actual construction of the device. The dashed line between drain and source was chosen to reflect the fact that a channel does not exist between the two under no-bias conditions. It is, in fact, the only difference between the symbols for the depletion-type and enhancement-type MOSFETs.
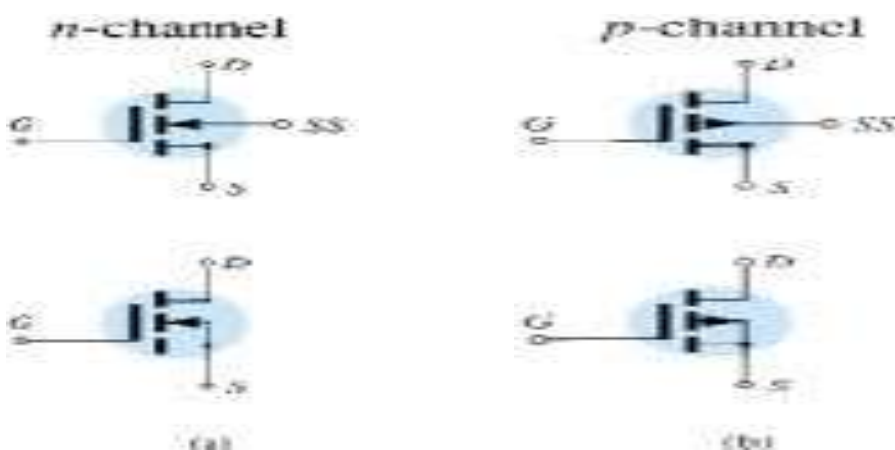
Fig 1.26 Symbols for (a) *n*-channel enhancement-type MOSFETs
(b) *p*-channel enhancement-type MOSFETs

<div align="center">

1.7 CMOS

</div>

A very effective logic circuit can be established by constructing a *p*-channel and an *n*-channel MOSFET on the same substrate as shown in Fig. 1.27. Note the induced *p*-channel on the left and the induced *n*-channel on the right for the *p*- and *n*-channel devices, respectively. The configuration is referred to as a *complementary MOSFET* arrangement (CMOS) that has extensive applications in computer logic design. The relatively high input impedance, fast switching speeds, and lower operating power levels of the CMOS configuration have resulted in a whole new discipline referred to as *CMOS logic design.*

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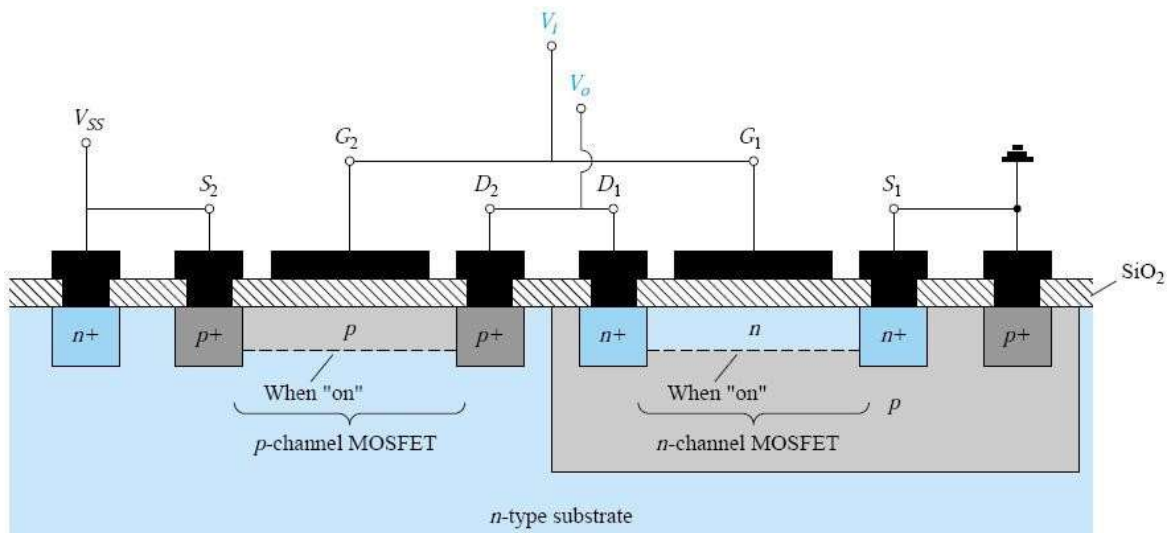
Fig 1.27 CMOS

</div>

One very effective use of the complementary arrangement is as an inverter, as shown in Fig. 1.28. As introduced for switching transistors, an inverter is a logic element that "inverts" the applied signal. That is, if the logic levels of operation are 0 V (0-state) and 5 V (1-state), an input level of 0 V will result in an output level of 5 V, and vice versa. Note in Fig. 1.28 that both gates are connected to the applied signal and both drain to the output V_o. The source of the *p*-channel MOSFET (Q_2) is connected directly to the applied voltage V_{SS}, while the source of the *n*-channel MOSFET (Q_1) is connected to ground. For the logic levels defined above, the application of 5 V at the input should result in approximately 0 V at the output. With 5 V at V_i (with respect to ground), V_{GS1} - V_i and Q_1 is "on," resulting in a relatively low resistance between drain and source as shown in Fig. 1.29. Since V_i and V_{SS} are at 5 V, V_{GS2} - 0 V, which is less than the required V_T for the device, resulting in an "off" state. The resulting resistance level between drain and source is quite high for Q_2, as shown in Fig. 1.29. A simple application of the voltage-divider rule will reveal that V_o is very close to 0 V or the 0-state, establishing the desired inversion process. For an applied voltage V_i of 0 V (0-state), V_{GS1} - 0 V and Q_1 will be off with V_{SS2} = -5 V, turning

on the p-channel MOSFET. The result is that Q_2 will present a small

resistance level, Q_1 a high resistance, and $V_o = V_{SS} = 5$ V (the 1-state). Since the drain current that flows for either case is limited by the "off" transistor to the leakage value, the power dissipated by the device in either state is very low.
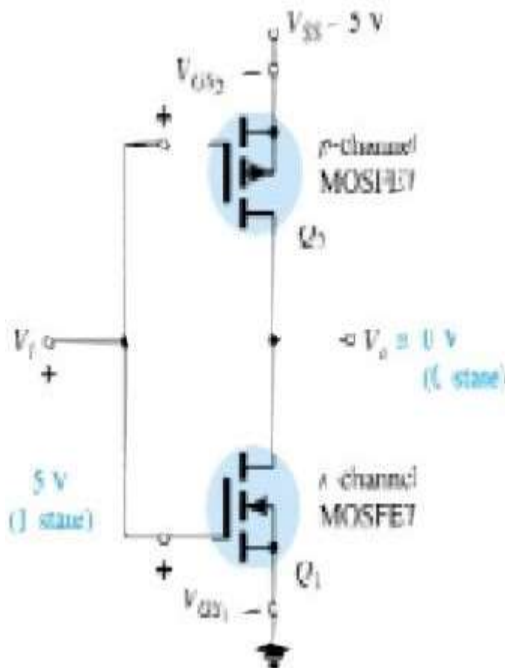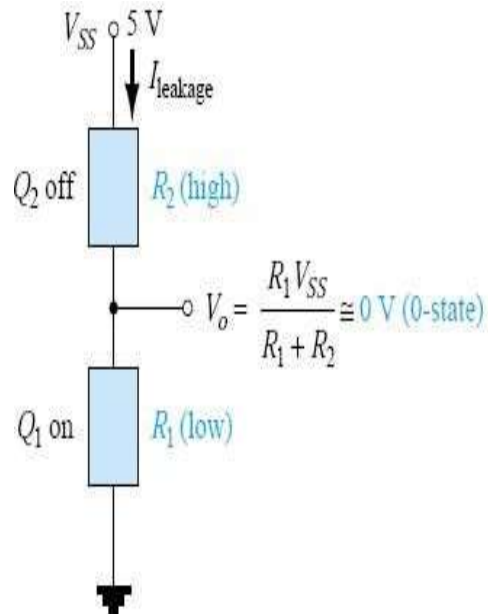

Fig 1.28 CMOS inverter   Fig 1.29 Relative resistance levels for $V_i = 5$ V

<u>**Chapter 2 BIASING OF BJTS**</u>

2.1   INTRODUCTION

The analysis or design of a transistor amplifier requires knowledge of both the dc and ac response of the system. Too often it is assumed that the transistor is a magical device that can raise the level of the applied ac input without the assistance of an external energy source. In actuality, the improved output ac power level is the result of a transfer of energy from the applied dc supplies. The analysis or design of any electronic amplifier therefore has two components: the dc portion and the ac portion. Fortunately, the superposition theorem is applicable and the investigation of the dc conditions can be totally separated from the ac response. However, one must keep in mind that during the design or synthesis stage the choice of parameters for the required dc levels will affect the ac response, and vice versa.

The dc level of operation of a transistor is controlled by a number of factors, including the range of possible operating points on the device characteristics. Once the desired dc current and voltage levels have been defined, a network must be constructed that will establish the desired operating point. Each design will also determine the stability of the system, that is, how sensitive the system is to temperature variations.

Basic relationships for a transistor:

$$V_{BE} = 0.7V \text{ ----------------------------- (2.1)}$$
$$I_E = (1+ \beta)I_B = I_C \text{ ----------------------- (2.2)}$$
$$I_C = \beta I_B \text{ ----------------------------------- (2.3)}$$

In most instances the base current I_B is the first quantity to be determined. Once I_B is known, the relationships of Eqs. (2.1) through (2.3) can be applied to find the remaining quantities of interest.

2.2   OPERATING POINT

The term *biasing* appearing in the title of this chapter is an all-inclusive term for the application of dc voltages to establish a fixed level of current and voltage. For transistor amplifiers the resulting dc current and voltage establish an *operating point* on the characteristics that define the region that will be employed for amplification of the applied signal. Since the operating point is a fixed point on the characteristics, it is also called the *quiescent point* (abbreviated *Q*-point). By definition, *quiescent* means quiet, still, inactive. Figure 1.1 shows a general output device characteristic with four operating points indicated. The biasing circuit can be designed to set the device operation at any of these points or others within the *active region*. The maximum ratings are indicated on the characteristics of Fig. 1.1 by a horizontal line for the maximum collector current I_{Cmax} and a vertical line at the maximum collector-

to-emitter voltage V_{CEmax}. The maximum power constraint is defined by the curve P_{Cmax} in the same figure. At the lower end of the scales is the cut-off region, defined by $I_B \leq 0\mu A$, and the *saturation region*, defined by $V_{CE} \leq V_{CEsat}$.
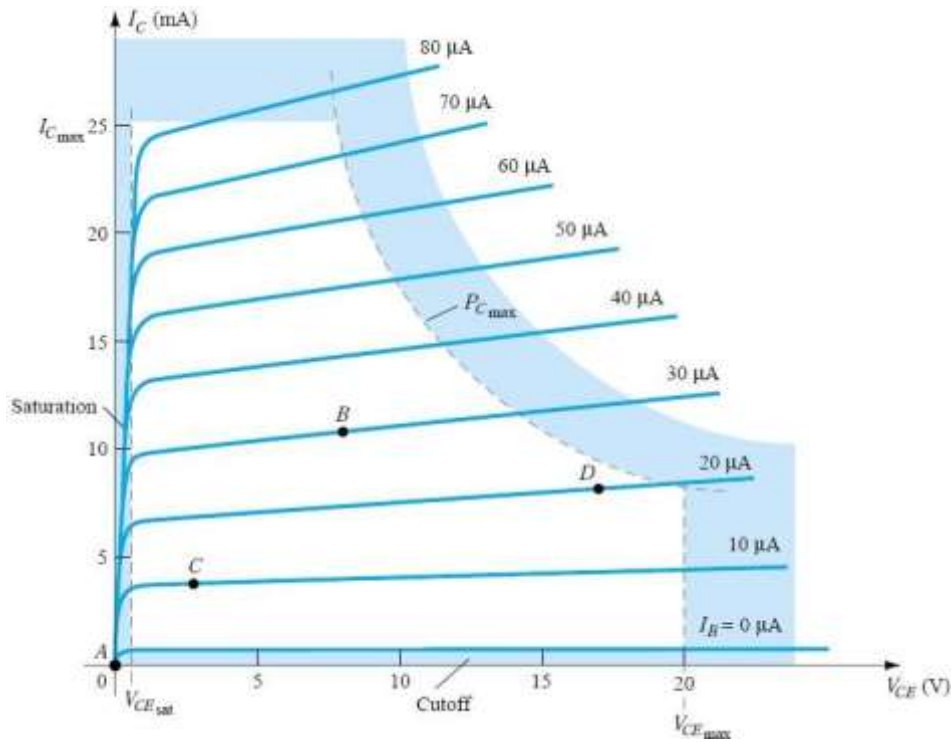

Fig 2.1 Various operating points within the limits of operation of a transistor

The BJT device could be biased to operate outside these maximum limits, but the result of such operation would be either a considerable shortening of the lifetime of the device or destruction of the device. Confining ourselves to the *active* region, one can select many different operating areas or points. The chosen *Q*-point often depends on the intended use of the circuit.

 If no bias were used, the device would initially be completely off, resulting in a *Q*-point at *A*—namely, zero current through the device (and zero voltage across it). Since it is necessary to bias a device so that it can respond to the entire range of an input signal, point *A* would not be suitable. For point *B*, if a signal is applied to the circuit, the device will vary in current and voltage from operating point, allowing the device to react to (and possibly amplify) both the positive and negative excursions of the input signal. If the input signal is properly chosen, the voltage and current of the device will vary but not enough to drive the device into *cut-off* or *saturation*. Point *C* would allow some positive and negative variation of the output signal, but the peak-to-peak value would be limited by the proximity of $V_{CE} = 0V/I_C = 0$ mA. Operating at point *C* also raises some concern about the nonlinearities introduced by the fact that the spacing between I_B curves is rapidly changing in this region. In general, it is preferable

to operate where the gain of the device is fairly constant (or linear) to ensure that the amplification over the entire swing of input signal is the same. Point *B* is a region of more linear spacing and therefore more linear operation, as shown in Fig. 2.1. Point *D* sets the device operating point near the maximum voltage and power level. The output voltage swing in the positive direction is thus limited if the maximum voltage is not to be exceeded. Point *B* therefore seems the best operating point in terms of linear gain and largest possible voltage and current swing. This is usually the desired condition for small-signal amplifiers but not the case necessarily for power amplifiers.

One other very important biasing factor must be considered. Having selected and biased the BJT at a desired operating point, the effect of temperature must also be taken into account. Temperature causes the device parameters such as the transistor current gain (β_{ac}) and the transistor leakage current (I_{CEO}) to change. Higher temperatures result in increased leakage currents in the device, thereby changing the operating condition set by the biasing network. The result is that the network design must also provide a degree of *temperature stability* so that temperature changes result in minimum changes in the operating point. This maintenance of the operating point can be specified by a *stability factor*, *S*, which indicates the degree of change in operating point due to a temperature variation. A highly stable circuit is desirable, and the stability of a few basic bias circuits will be compared.

For the BJT to be biased in its linear or active operating region the following must be true:
1. The *base–emitter junction must be forward-biased* (*p*-region voltage more *p*ositive), with a resulting forward-bias voltage of about 0.6to 0.7 V.
2. The *base–collector junction must be reverse-biased* (*n*-region more *p*ositive), with the reverse-bias voltage being any value within the maximum limits of the device.

[Note that for forward bias the voltage across the *p-n* junction is *p-p*ositive, while for reverse bias it is opposite (reverse) with *n-p*ositive.]

Operation in the cut-off, saturation, and linear regions of the BJT characteristic are provided as follows:

1. *Linear-region operation:* Base–
emitter junction forward biased Base–
collector junction reverse biased

2. *Cut-off-region operation:*
Base–emitter junction reverse biased

3. *Saturation-region operation:* Base–
emitter junction forward biased Base–
collector junction forward biased

2.3   FIXED-BIAS CIRCUIT

The fixed-bias circuit of Fig. 2.2 provides a relatively straightforward and simple introduction to transistor dc bias analysis. Even though the network employs an *npn* transistor, the equations and calculations apply equally well to a *pnp* transistor configuration merely by changing all current directions and voltage polarities. The current directions of Fig. 2.2 are the actual current directions, and the voltages are defined by the standard double-subscript notation. For the dc analysis the network can be isolated from the indicated ac levels by replacing the capacitors with an open circuit equivalent. In addition, the dc supply V_{CC} can be separated into two supplies (for analysis purposes only) as shown in Fig. 2.3 to permit a separation of input and output circuits. It also reduces the linkage between the two to the base current I_B. The separation is certainly valid, as we note in Fig. 2.3 that V_{CC} is connected directly to R_B and R_C just as in Fig. 2.2.
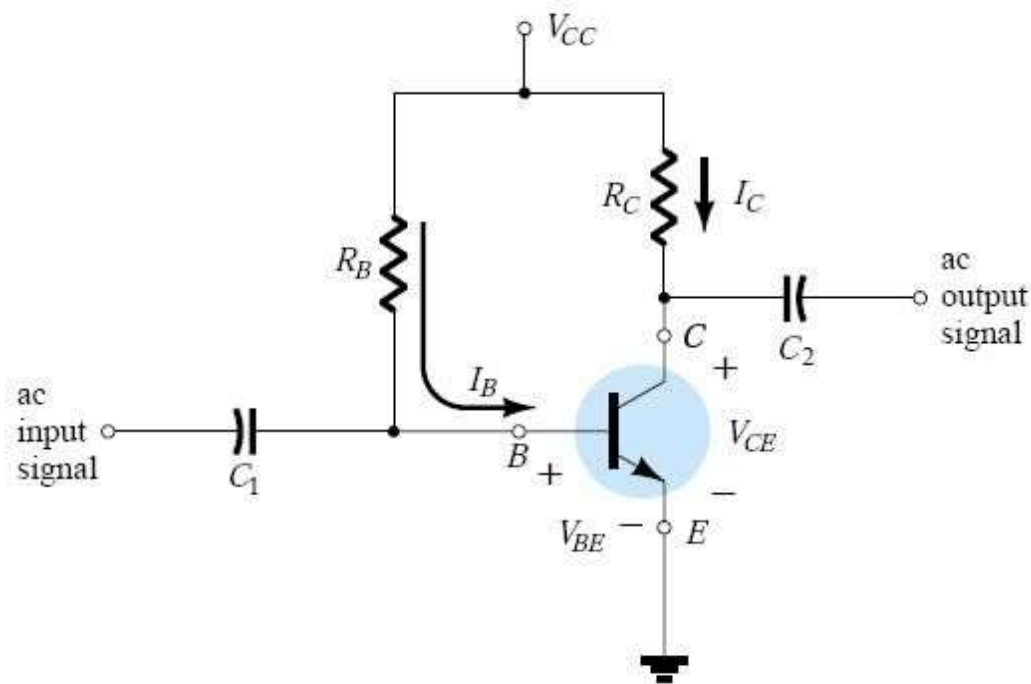
Fig 2.2 Fixed-bias circuit
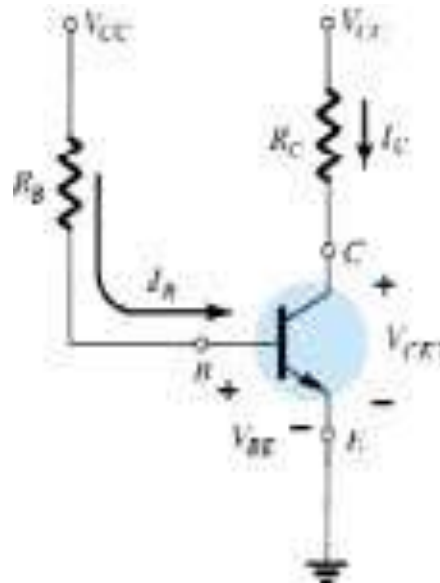
Fig 2.3 dc equivalent of Fig. 2.2

Base-Emitter Loop

Consider first the base–emitter circuit loop of Fig. 1.4. Writing Kirchhoff's voltage equation in the clockwise direction for the loop, we obtain

$+V_{CC} - I_B R_B - V_{BE} = 0$

Solving the equation for the current I_B will result in the following:
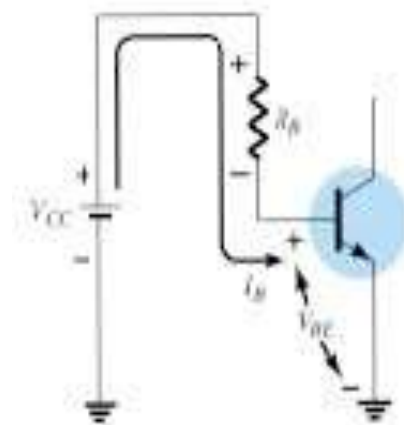
$$\mathbf{I_B = (V_{BE} - V_{CC})/R_B} \text{-------------------------}(2.4)$$

Fig 2.4 Base–emitter loop

Collector–Emitter Loop

Applying Kirchhoff's voltage law in the clockwise direction around the indicated collector – emitter closed loop of Fig. 2.5 will result in the following:

$V_{CE} + I_C R_C - V_{CC} = 0$

Solving the equation for the voltage V_{CE} will result in the following:

$$\mathbf{V_{CE} = V_{CC} - I_C R_C} \text{ ----------------------------- (2.5)}$$
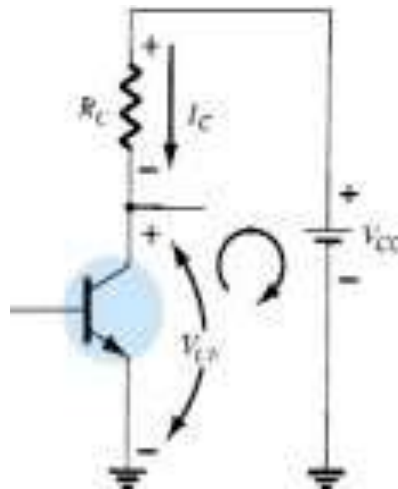
Fig 2.5 Collector–emitter loop

Keep in mind, $\mathbf{I_C = \beta I_B,\ V_{CE} = V_C - V_E,\ V_{BE} = V_B - V_E}$

Transistor Saturation

The term *saturation* is applied to any system where levels have reached their maximum values. For a transistor operating in the saturation region, the current is a maximum value *for the particular design.* Change the design and the corresponding saturation level may rise or drop. Of course, *the highest saturation level is defined by the maximum collector current as provided by the specification sheet*.
Saturation conditions are normally avoided because the base–collector junction is no longer reverse-biased and the output amplified signal will be distorted.

The resulting saturation current for the fixed-bias configuration is

$$\mathbf{I_{Csat} = V_{CC}/R_C} \text{ --------------------- (2.6)}$$

Once I_{Csat} is known, we have some idea of the maximum possible collector current for the chosen design and the level to stay below if we expect linear amplification.

Load-Line Analysis

The network of Fig. 2.6(a) establishes an output equation that relates the variables I_C and V_{CE} in the following manner:
$V_{CE} = V_{CC} - I_C R_C$ ------------------- (2.7)

The output characteristics of the transistor also relate the same two variables I_C and V_{CE} as shown in Fig. 2.6(b).
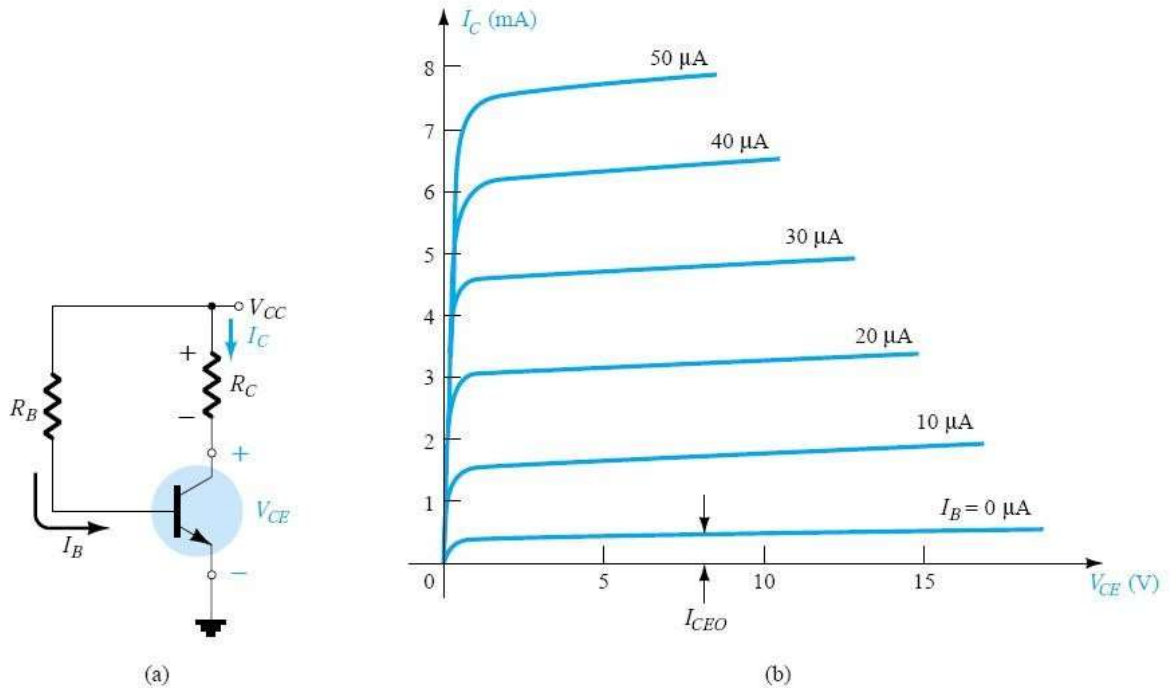

Fig 2.6 Load-line analysis: (a) the network; (b) the device characteristics

The common solution of the two occurs where the constraints established by each are satisfied simultaneously. In other words, this is similar to finding the solution of two simultaneous equations: one established by the network and the other by the device characteristics.

The device characteristics of I_C versus V_{CE} are provided in Fig. 2.6(b). We must now superimpose the straight line defined by Eq. (2.7) on the characteristics. The most direct method of plotting Eq. (2.7) on the output characteristics is to use the fact that a straight line is defined by two points.

$$\mathbf{V_{CE} = V_{CC}|I_C = 0mA} \text{ ------------------- (2.8)}$$

$$\mathbf{I_C = (V_{CC}/R_C)|V_{CE} = 0V} \text{ --------------- (2.9)}$$

By joining the two points defined by Eqs. (2.8) and (2.9), the straight line established by Eq. (2.8) can be drawn. The resulting line on the graph of Fig. 2.7 is called the *load line* since it is defined by the load resistor R_C. By solving for the resulting level of I_B, the actual Q-point can be established as shown in Fig. 2.7.
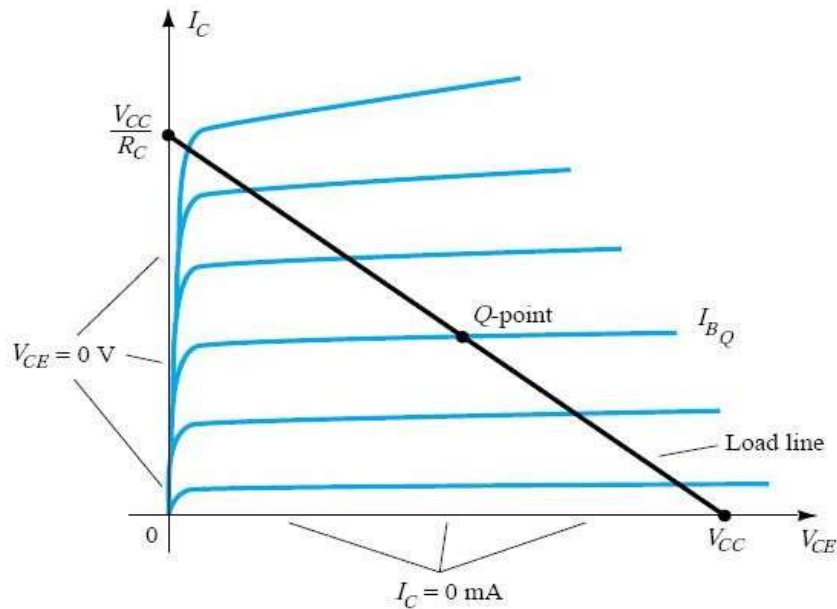
Fig 2.7 Fixed-bias load line

2.4   EMITTER-STABILIZED BIAS CIRCUIT

The dc bias network of Fig. 2.8 contains an emitter resistor to improve the stability level over that of the fixed-bias configuration.
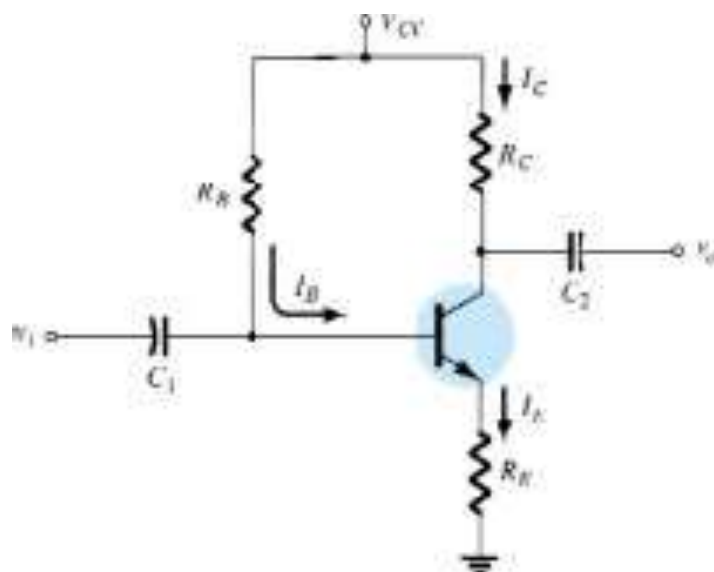
Fig 2.8 BJT bias circuit with emitter resistor

Base–Emitter Loop

The base–emitter loop of the network of Fig. 2.8 can be redrawn as shown in Fig.2.9. Writing Kirchhoff's voltage law around the indicated loop in the clockwise direction will result in the following equation:

$+V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$ ----------------------(2.10)

Substituting for $I_E = (1+\beta)I_B$ in Eq. (2.10) and solving for I_B gives,

$$\mathbf{I_B = (V_{CC} - V_{BE})/[R_B + (1+\beta)R_E]}\text{-------------- (2.11)}$$
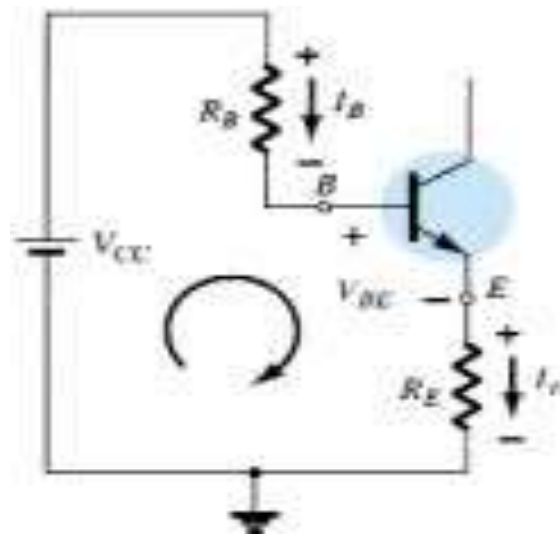
Fig 2.9 Base–emitter loop

Note that: *The only difference between this equation for I_B and that obtained for the fixed-bias configuration is the term $(1+\beta)R_E$.*

Collector–Emitter Loop

The collector–emitter loop is redrawn. Writing Kirchhoff's voltage law for the indicated loop in the clockwise direction will result in:

$+I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$-------------------- (2.11)

Substituting $I_E = I_C$ and grouping terms gives,

$$\mathbf{V_{CE} = V_{CC} - I_C(R_C + R_E)}\text{------------------- (2.12)}$$

Keep in mind,
$\mathbf{V_E = I_E R_E}$
$\mathbf{V_C = V_{CE} + V_E = V_{CC} - I_C R_C}$
$\mathbf{V_B = V_{BE} + V_E = V_{CC} - I_B R_B}$

Improved Bias Stability

The *addition of the emitter resistor to the dc bias of the BJT provides improved stability*, that is, the dc bias currents and voltages remain closer to where they were set by the circuit when outside conditions, such as temperature, and transistor beta, change.

Saturation Level

The collector saturation level or maximum collector current for an emitter-bias design can be determined using the same approach applied to the fixed-bias configuration:

$$\mathbf{I_{Csat} = V_{CC}/(R_C + R_E)} \text{ ------------------------ (2.13)}$$

The addition of the emitter resistor reduces the collector saturation level below that obtained with a fixed-bias configuration using the same collector resistor.

Load-Line Analysis

The load-line analysis of the emitter-bias network is only slightly different from that encountered for the fixed-bias configuration.
The collector–emitter loop equation that defines the load line is the following:
$V_{CE} = V_{CC} - I_C(R_C + R_E)$ ------------------ (2.14)

The most direct method of plotting Eq. (2.14) on the output characteristics is to use the fact that a straight line is defined by two points.

$$\mathbf{V_{CE} = V_{CC}|I_C = 0mA} \text{ ----------------------------(2.15)}$$
$$\mathbf{I_C = V_{CC}/(R_C + R_E)|V_E = 0V} \text{ -----------------(2.16)}$$
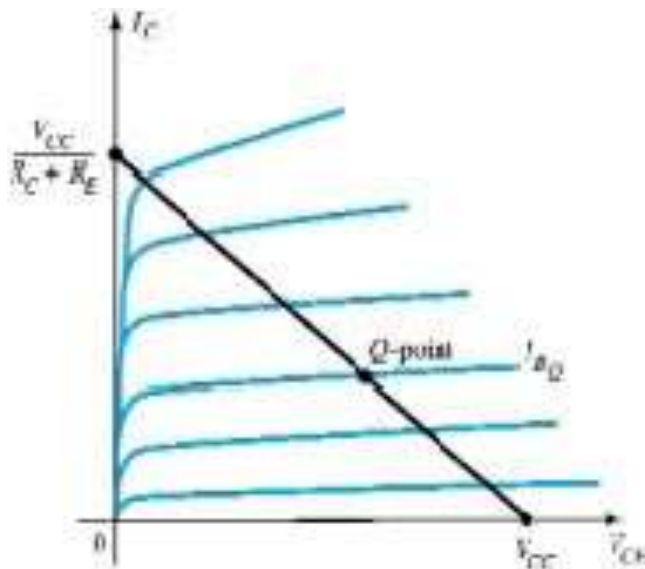
Fig 2.10 Load line for the emitter-bias configuration

<u>2.5</u>   <u>VOLTAGE-DIVIDER BIAS</u>

In the previous bias configurations the bias current I_{CQ} and voltage V_{CEQ} were a function of the current gain (β) of the transistor. However, since β is temperature sensitive, especially for silicon transistors, and the actual value of beta is usually not well defined, it would be desirable to develop a bias circuit that is less dependent, or in fact, independent of the transistor beta. The voltage-divider bias configuration of Fig. 2.11 is such a network. If analyzed on an exact basis the sensitivity to changes in beta is quite small. If the circuit parameters are properly chosen, the resulting levels of I_{CQ} and V_{CEQ} can be almost totally independent of beta.
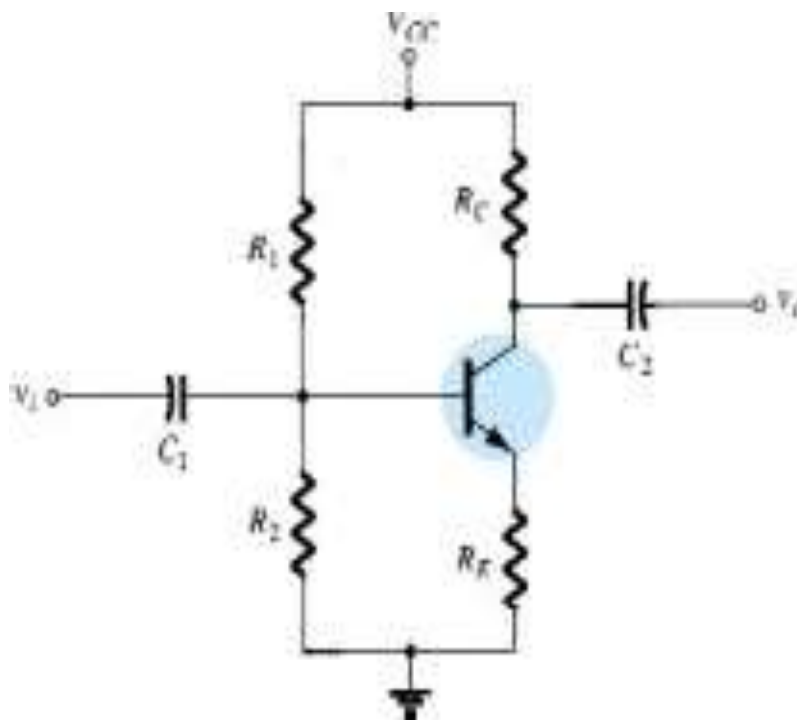
Fig 2.11 Voltage-divider bias configuration

There are two methods that can be applied to analyze the voltage-divider configuration. The first to be demonstrated is the *exact method* that can be applied to *any* voltage-divider configuration. The second is referred to as the *approximate method* and can be applied only if specific conditions are satisfied. The approximate approach permits a more direct analysis with a savings in time and energy.
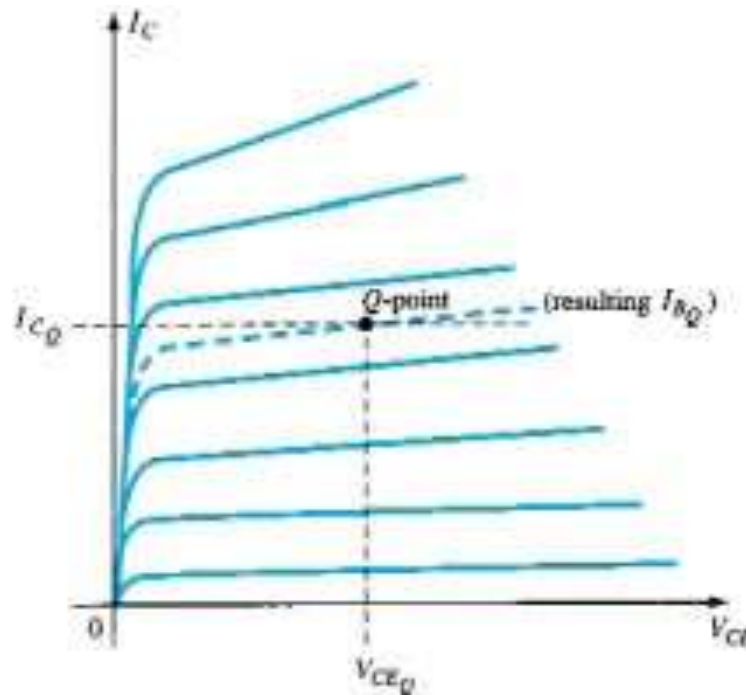
Fig 2.12 Defining the Q-point for the voltage-divider bias configuration

Exact Analysis

The input side of the network of Fig. 2.11 can be redrawn as shown in Fig. 2.13 for the dc analysis. The Thévenin equivalent network for the network to the left of the base terminal can then be found in the following manner:
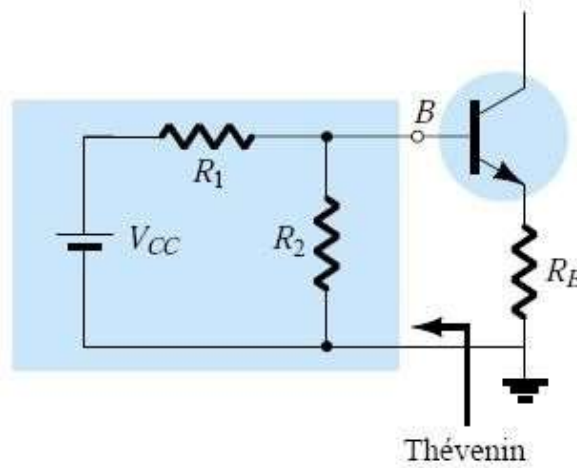

Thévenin

Fig 2.13 Redrawing the input side of the network of Fig. 2.11

$R_{th} = R_1 \| R_2$ -------------------------------- (2.17)

$E_{th} = V_{R2} = V_{CC}R_2/(R_1+R_2)$ --------------- (2.18)
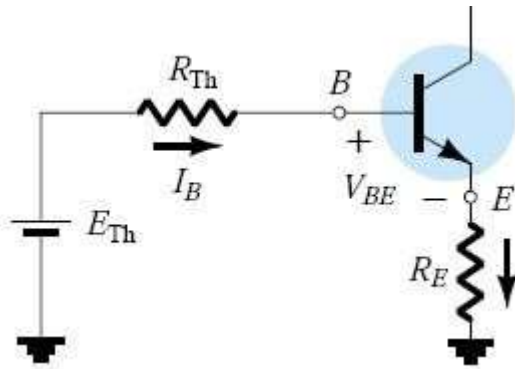
Fig 2.14 Inserting the Thévenin equivalent circuit

The Thévenin network is then redrawn as shown in Fig. 2.14, and I_{BQ} can be determined by first applying Kirchhoff's voltage law in the clockwise direction for the loop indicated:

$E_{Th} - I_B R_{Th} - V_{BE} - I_E R_E = 0$

i.e. **$I_B = (E_{Th} - V_{BE})/R_{Th} + (1+\beta)R_E$** ------- (2.19)

Solving for V_{CE} in the collector-emitter loop,

$V_{CE} = V_{CC} - I_C(R_C+R_E)$ ----------------------(2.20)

Approximate Analysis

The input section of the voltage-divider configuration can be represented by the network of Fig. 2.15. The resistance R_i is the equivalent resistance between base and ground for the transistor with an emitter resistor R_E. The reflected resistance between base and emitter is defined by $R_i = (\beta+1)R_E$. If R_i is much larger than the resistance R_2, the current I_B will be much smaller than I_2 (current always seeks the path of least resistance) and I_2 will be approximately equal to I_1. If we accept the approximation that I_B is essentially zero amperes compared to I_1 or I_2, then $I_1 = I_2$ and R_1 and R_2 can be considered series elements.
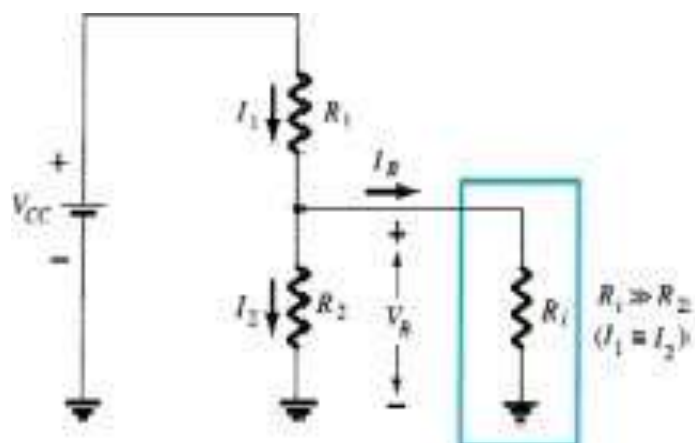
Fig 2.15 Partial-bias circuit for calculating the approximate base voltage V_B

The voltage across R_2, which is actually the base voltage, can be determined using the voltage-divider rule.

$$\mathbf{V_B = V_{CC}R_2/(R_1+R_2)} \text{-------------------------------- (2.21)}$$

Since $Ri = (\beta + 1)R_E = \beta R_E$ the condition that will define whether the approximate approach can be applied will be the following:

$$\mathbf{\beta R_E \geq 10R_2} \text{----------------------------------- (2.22)}$$

In other words, if β times the value of R_E is at least 10 times the value of R_2, the approximate approach can be applied with a high degree of accuracy.

Once V_B is determined,

$$\mathbf{V_E = V_B - V_{BE}} \text{-------------------------------------(2.23)}$$
$$\mathbf{I_E = V_E/R_E} \text{--- (2.24)}$$
$$\mathbf{I_{CQ} = I_E} \text{---(2.25)}$$
$$\mathbf{V_{CEQ} = V_{CC} - I_C(R_C+R_E)} \text{---------------------- (2.26)}$$

Note in the sequence of calculations from Eq. (2.21) through Eq. (2.26) that β does not appear and I_B was not calculated. The Q-point (as determined by I_{CQ} and V_{CEQ}) is therefore independent of the value of β.

Transistor Saturation

The output collector–emitter circuit for the voltage-divider configuration has the same appearance as the emitter-biased circuit analyzed in Section 2.4. The resulting equation for the saturation current is therefore the same as obtained for the emitter-biased configuration. That is,

$$\mathbf{I_{Csat} = I_{Cmax} = V_{CC}/(R_C + R_E)} \text{----------------------------- (2.28)}$$

Load-Line Analysis

The similarities with the output circuit of the emitter-biased configuration result in the same intersections for the load line of the voltage-divider configuration.

$$\mathbf{I_C = V_{CC}/(R_C+R_E)|V_{CE}=0V} \text{--------------------- (2.29)}$$
$$\mathbf{V_{CE} = V_{CC}|I_C=0mA} \text{----------------------------- (2.30)}$$

The level of I_B is of course determined by a different equation for the voltage-divider bias and the emitter-bias configurations.

2.6   DC BIAS WITH VOLTAGE FEEDBACK

An improved level of stability can also be obtained by introducing a feedback path from collector to base as shown in Fig. 1.16. Although the *Q*-point is not totally independent of beta (even under approximate conditions), the sensitivity to changes in beta or temperature variations is normally less than encountered for the fixed-bias or emitter-biased configurations.
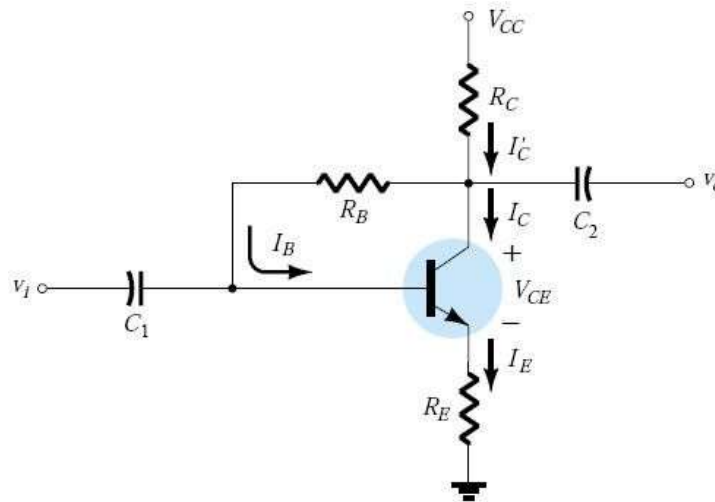

Fig 2.16 dc bias circuit with voltage feedback

Base–Emitter Loop

Fig 2.17 shows the base–emitter loop for the voltage feedback configuration. Writing Kirchhoff's voltage law around the indicated loop in the clockwise direction will result in

$V_{CC} - I_C'R_C - I_BR_B - V_{BE} - I_ER_E = 0$

Putting $I_{C'} = \beta I_B$ and solving for I_B gives,

$$\mathbf{I_B = (V_{CC} - V_{BE})/[R_B + \beta(R_C + R_E)]} \text{---------------------} (2.31)$$
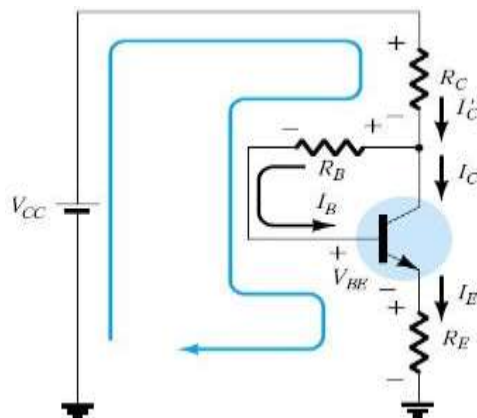
Fig 2.17 Base–emitter loop for the network of Fig. 2.16

Collector–Emitter Loop

The collector–emitter loop for the network of Fig. 2.16 is provided in Fig. 2.18. Applying Kirchhoff's voltage law around the indicated loop in the clockwise direction will result in
$I_E R_E + V_{CE} + I_{C'} R_C - V_{CC} = 0$

Since $I_{C'} = I_C = I_E$ and solving for V_{CE} gives,
$$\mathbf{V_{CE} = V_{CC} - I_C(R_C + R_E)} \text{------------------------} (2.32)$$
which is exactly as obtained for the emitter-bias and voltage-divider bias configurations.
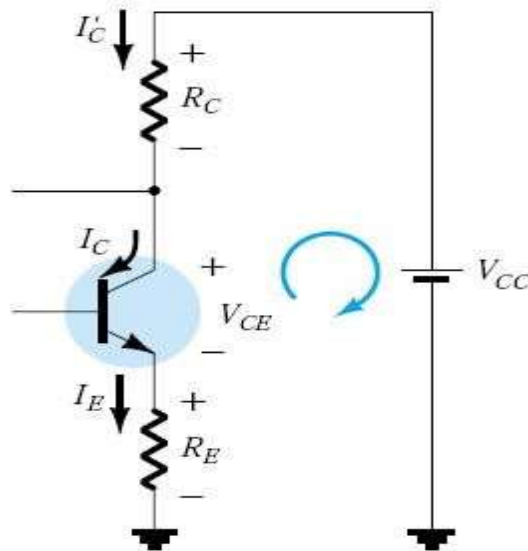
Fig 2.18 Collector–emitter loop for the network of Fig. 2.16

Saturation Conditions

Using the approximation $I'_C = I_C$, the equation for the saturation current is the same as obtained for the voltage-divider and emitter-bias configurations. That is,

$$\mathbf{I_{Csat} = I_{Cmax} = V_{CC}/(R_C + R_E)} \text{--------------------------} (2.33)$$

Load-Line Analysis

Continuing with the approximation $I'_C = I_C$ will result in the same load line defined for the voltage-divider and emitter-biased configurations. The level of I_{BQ} will be defined by the chosen bias configuration.

<u>2.7</u>   <u>BIAS STABILIZATION</u>

The stability of a system is a measure of the sensitivity of a network to variations in its parameters. In any amplifier employing a transistor the collector current I_C is sensitive to each of the following parameters:

β: *increases with increase in temperature*
|V_{BE}|: *decreases about 7.5 mV per degree Celsius (°C) increase in temperature*
I_{CO} (reverse saturation current): doubles in value for every 10°C increase in Temperature

<u>Stability Factors, $S(I_{CO})$, $S(V_{BE})$, and $S(β)$</u>

A stability factor, *S*, is defined for each of the parameters affecting bias stability as listed below:

$S(I_{CO}) = \Delta I_C / \Delta I_{CO}$ --------------------------(2.34)

$S(V_{BE}) = \Delta I_C / \Delta V_{BE}$ ------------------------(2.35)

$S(β) = \Delta I_C / β$ -------------------------------(2.36)

In each case, the delta symbol (Δ) signifies change in that quantity. The numerator of each equation is the change in collector current as established by the change in the quantity in the denominator. For a particular configuration, if a change in I_{CO} fails to produce a significant change in I_C, the stability factor defined by $S(I_{CO}) = \Delta I_C / \Delta I_{CO}$ will be quite small. In other words:
Networks that are quite stable and relatively insensitive to temperature variations have low stability factors.
The higher the stability factor, the more sensitive the network to variations in that parameter.

<u>$S(I_{CO})$: EMITTER-BIAS CONFIGURATION</u>

For the emitter-bias configuration, an analysis of the network will result in
        $S(I_{CO}) = (1+β)[(1+ R_B/R_E) / \{(β+1) + R_B/R_E\}]$ -----------------(2.37)

For $R_B/R_E >> (β+1)$, Eq. (1.37) will reduce to the following:
        $S(I_{CO}) = (1+β)$ ----------------------------(2.38)
For $R_B/R_E <<1$,
          $S(I_{CO}) = 1$ ----------------------------- (2.39)
For the range where R_B/R_E ranges between 1 and $(β+1)$,
        $S(I_{CO}) = R_B/R_E$ ------------------------------(2.40)

The results reveal that the emitter-bias configuration is quite stable when the ratio R_B/R_E is as small as possible and the least stable when the same ratio approaches $(\beta+1)$.

Fixed-Bias Configuration

$$\mathbf{S(I_{CO}) = (\beta+1)} \text{ -- (2.41)}$$

The result is a configuration with a poor stability factor and a high sensitivity to variations in I_{CO}.

Voltage-Divider Bias Configuration

$$\mathbf{S(ICO) = (1+\beta)[(1+ R_{Th}/R_E) / \{(\beta+1) + R_{Th}/R_E\}]} \text{ ------------------- (2.42)}$$

Feedback-Bias Configuration

$$\mathbf{S(I_{CO}) = (1+\beta)[(1+ R_B/R_C) / \{(\beta+1) + R_B/R_C\}]} \text{ ------------------------- (2.43)}$$

S(V_{BE}): EMITTER-BIAS CONFIGURATION

$$\mathbf{S(V_{BE}) = -\beta/[R_B + (1+\beta)R_E] = -(\beta/R_E)/[(R_B/R_E) + (1+\beta)]} \text{ --------------- (2.44)}$$

Fixed-Bias Configuration ($R_E = 0\Omega$)

$$\mathbf{S(V_{BE}) = -\beta/R_B} \text{ ------------------------------------- (2.45)}$$

For $(1+\beta) \gg RB/RE$,

$$\mathbf{S(V_{BE}) = -1/R_E} \text{ ------------------------------------ (2.46)}$$

revealing that the larger the resistance R_E, the lower the stability factor and the more stable the system.

S(β): EMITTER-BIAS CONFIGURATION

$$\mathbf{S(\beta) = [I_{C1}(1+R_B/R_E) / \{\beta_1(1+\beta_2+R_B/R_E)\}]} \text{ ------------- (2.46)}$$

The notation I_{C1} and $\beta 1$ is used to define their values under one set of network conditions, while the notation $\beta 2$ is used to define the new value of beta as established by such causes as temperature change, variation in β for the same transistor, or a change in transistors.

<u>Fixed-Bias Configuration($R_E = 0\Omega$)</u>

$$S(\beta) = [I_{C1}(R_B + R_C) / \beta_1\{R_B + R_C (1+\beta_2)\}]\text{-----------------------} (2.47)$$

<u>Summary</u>

Now that the three stability factors of importance have been introduced, the total effect on the collector current can be determined using the following equation:

$$\Delta I_C = S(I_{CO})\Delta I_{CO} + S(V_{BE})\Delta V_{BE} + S(\beta)\Delta\beta \text{ ------------------------} (2.48)$$

The equation may initially appear quite complex, but take note that each component is simply a stability factor for the configuration multiplied by the resulting change in a parameter between the temperature limits of interest. In addition, the ΔI_C to be determined is simply the change in IC from the level at room temperature.

For instance, if we examine the fixed-bias configuration, Eq. (2.48) becomes the following:

$$\Delta I_C = (\beta+1)\Delta I_{CO} + (-\beta/R_B)\Delta V_{BE} + (I_{C1}/\beta_1)\Delta\beta$$

The effect of $S(I_{CO})$ in the design process is becoming a lesser concern because of improved manufacturing techniques that continue to lower the level of $I_{CO} = I_{CBO}$. It should also be mentioned that for a particular transistor the variation in levels of I_{CBO} and V_{BE} from one transistor to another in a lot is almost negligible compared to the variation in beta. In addition, the results of the analysis above support the fact that for a good stabilized design:

The ratio R_B/R_E or R_{Th}/R_E should be as small as possible with due consideration to all aspects of the design, including the ac response.

Chapter 3 BIASING OF FETS AND MOSFETS

3.1   INTRODUCTION

For the *field-effect transistor (FET)*, the relationship between input and output quantities is *nonlinear* due to the squared term in Shockley's equation. Linear relationships result in straight lines when plotted on a graph of one variable versus the other, while non-linear functions result in curves as obtained for the transfer characteristics of a JFET. The non-linear relationship between I_D and V_{GS} can complicate the mathematical approach to the dc analysis of FET configurations. A graphical approach may limit solutions to tenths-place accuracy, but it is a quicker method for most FET amplifiers.

Whereas in *bipolar junction transistor (BJT)*, the biasing level can be obtained using the characteristic equations $V_{BE} = 0.7V$, $I_C = \beta I_B$, and $I_C = I_E$. The linkage between input and output variables is provided by β, which is assumed to be fixed in magnitude for the analysis to be performed. The fact that beta is a constant establishes a *linear* relationship between I_C and I_B. Doubling the value of I_B will double the level of I_C, and so on.

Another distinct difference between the analysis of BJT and FET transistors is that the input controlling variable for a BJT transistor is a current level, while for the FET a voltage is the controlling variable. In both cases, however, the controlled variable on the output side is a current level that also defines the important voltage levels of the output circuit.

The general relationships that can be applied to the dc analysis of all FET amplifiers are:

$$\mathbf{I_G = 0A} \text{ ---------------------------- (3.1)}$$
$$\mathbf{I_D = I_S} \text{----------------------------- (3.2)}$$

For JFETS and depletion-type MOSFETs, Shockley's equation is applied to relate the input and output quantities:

$$\mathbf{I_D = I_{DSS}(1 - V_{GS}/V_P)^2} \text{ -------------- (3.3)}$$

For enhancement-type MOSFETs, the following equation is applicable:

$$\mathbf{I_D = k(V_{GS} - V_T)^2} \text{ ----------------- (3.4)}$$

3.2   FIXED-BIAS CONFIGURATION

The simplest of biasing arrangements for the *n*-channel JFET appears in Fig. 3.1. The fixed-bias configuration is one of the few FET configurations that can be solved just as directly using either a mathematical or graphical approach. The configuration of Fig. 3.1 includes the ac levels V_i and V_o and the coupling capacitors (C_1 and C_2). The coupling capacitors are "open circuits" for the dc analysis and low impedances (essentially short circuits) for the ac analysis. The resistor R_G is present to ensure that V_i appears at the input to the FET amplifier for the ac analysis.

For the dc analysis,

$I_G = 0A$ and $V_{RG} = I_G R_G = (0A)R_G = 0V$

The zero-volt drop across R_G permits replacing R_G by a short-circuit equivalent, as appearing in the network of Fig. 3.2 specifically redrawn for the dc analysis.
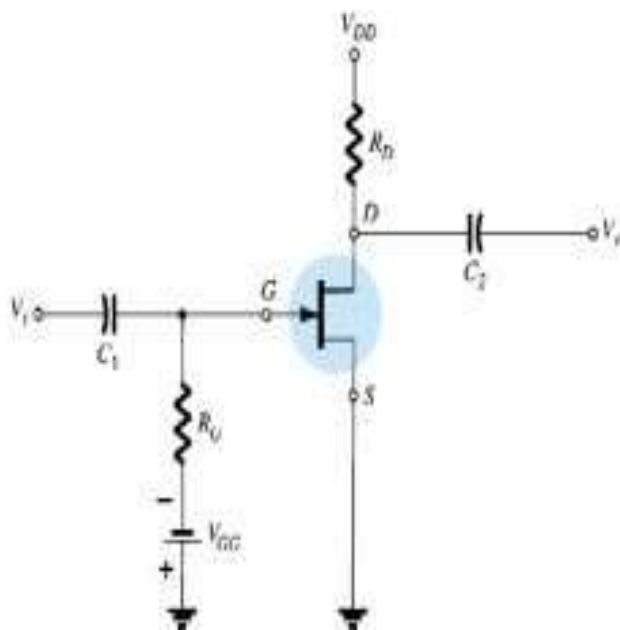
Fig 3.1 Fixed-bias configuration   Fig 3.2 Network for dc analysis
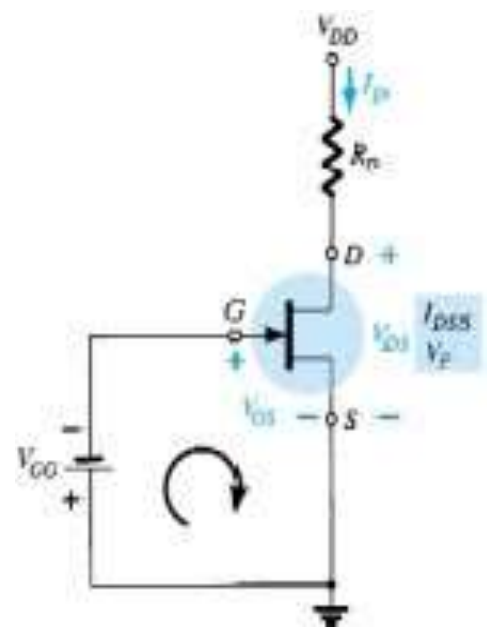
The fact that the negative terminal of the battery is connected directly to the defined positive potential of V_{GS} clearly reveals that the polarity of V_{GS} is directly opposite to that of V_{GG}. Applying Kirchhoff's voltage law in the clockwise direction of the indicated loop of Fig. 3.2 will result in:

$$\textbf{V}_{\textbf{GS}} = \textbf{-V}_{\textbf{GG}}\text{---------------------------------} (3.5)$$

Since V_{GG} is a fixed dc supply, the voltage V_{GS} is fixed in magnitude, resulting in the notation "fixed-bias configuration."

The resulting level of drain current I_D is now controlled by Shockley's equation:
$$I_D = I_{DSS}(1-V_{GS}/V_P)^2$$
Since V_{GS} is a fixed quantity for this configuration, its magnitude and sign can simply be substituted into Shockley's equation and the resulting level of I_D calculated.

A graphical analysis would require a plot of Shockley's equation as shown in Fig. 3.3. Choosing $V_{GS}= V_P/2$ will result in a drain current of $I_{DSS}/4$ when plotting the equation. For the analysis of this chapter, the three points defined by I_{DSS}, V_P, and the intersection just described will be sufficient for plotting the curve.
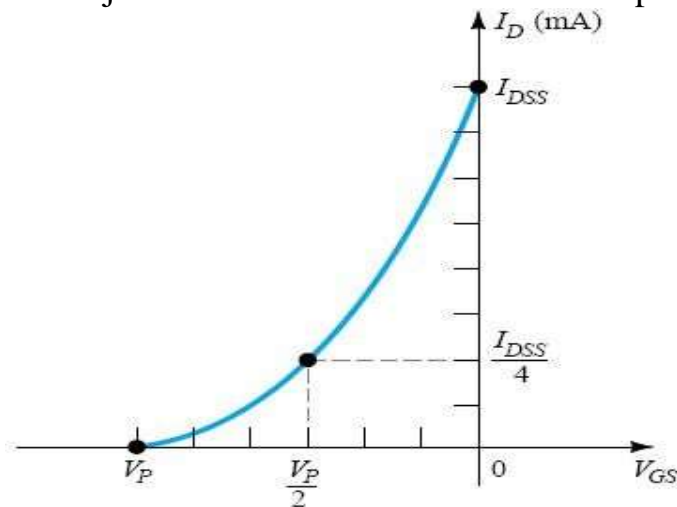
Fig 3.3 Plotting Shockley's equation

In Fig. 3.4, the fixed level of V_{GS} has been superimposed as a vertical line at $V_{GS} = -V_{GG}$. At any point on the vertical line, the level of V_{GS} is $-V_{GG}$—the level of I_D must simply be determined on this vertical line. The point where the two curves intersect is the common solution to the configuration—commonly referred to as the *quiescent* or *operating point or Q-point.*
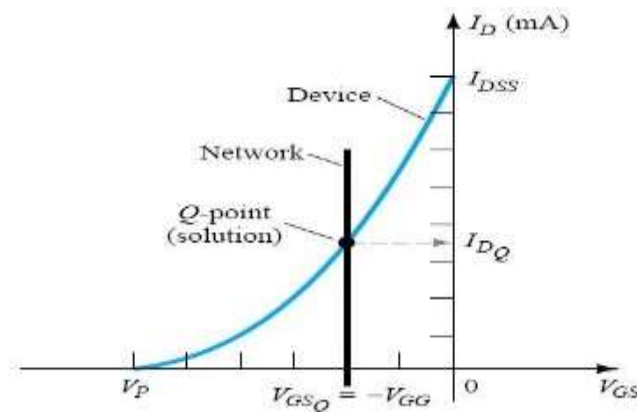
Fig 3.4 Finding the solution for the fixed-bias configuration

The drain-to-source voltage of the output section can be determined by applying Kirchhoff's voltage law as follows:

$+V_{DS} + I_D R_D - V_{DD} = 0$

$$\text{Or, } \mathbf{V_{DS} = V_{DD} - I_D R_D} \text{ ----------------------------- (3.6)}$$

Keep in mind, $\mathbf{V_S = 0V}$ -------------------------------(3.7)

$$\mathbf{V_D = V_{DS}} \text{ ---------------------------- (3.8)}$$

$$\mathbf{V_G = V_{GS}} \text{ --------------------------(3.9)}$$

Since the configuration requires two dc supplies, its use is limited.

3.3   SELF-BIAS CONFIGURATION

The self-bias configuration eliminates the need for two dc supplies. The controlling gate-to-source voltage is now determined by the voltage across a resistor R_S introduced in the source leg of the configuration as shown in Fig. 3.5.
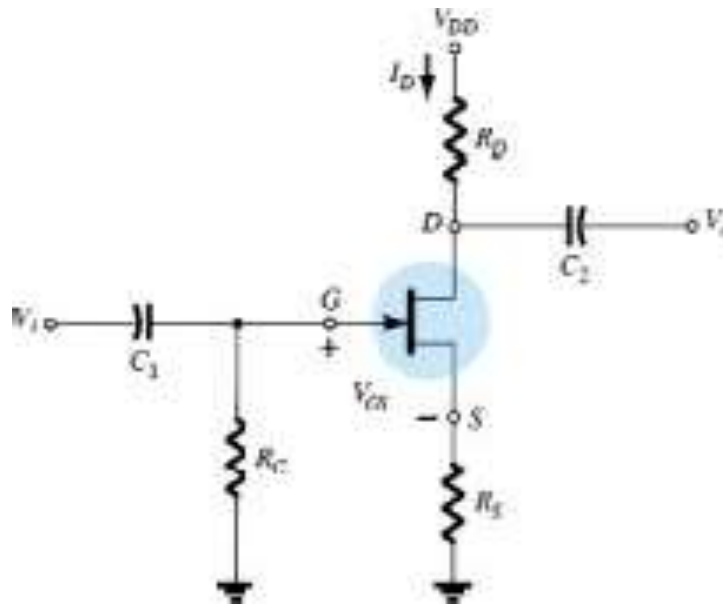
Fig 3.5 JFET self-bias configuration

For the dc analysis, the capacitors can again be replaced by "open circuits" and the resistor R_G replaced by a short-circuit equivalent since $I_G = 0$ A. The result is the network of Fig. 3.6 for the important dc analysis.
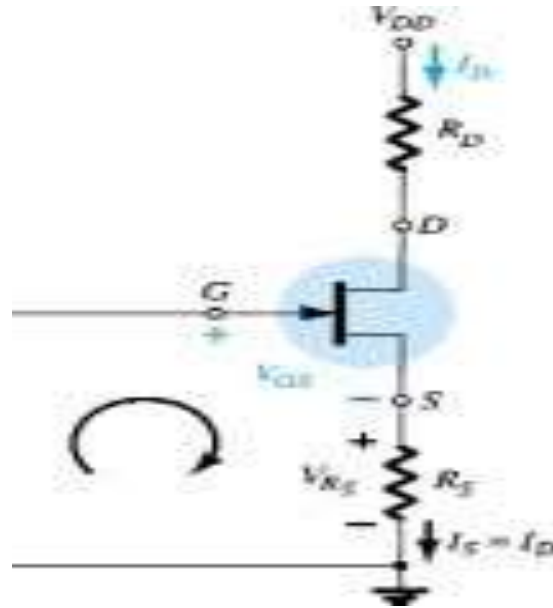
Fig 3.6 DC analysis of the self-bias configuration

For the indicated closed loop of Fig. 3.6, we find that
$V_{GS} = -I_D R_S$ ------------------(3.10)

Note in this case that V_{GS} is a function of the output current I_D and not fixed in magnitude as occurred for the fixed-bias configuration.
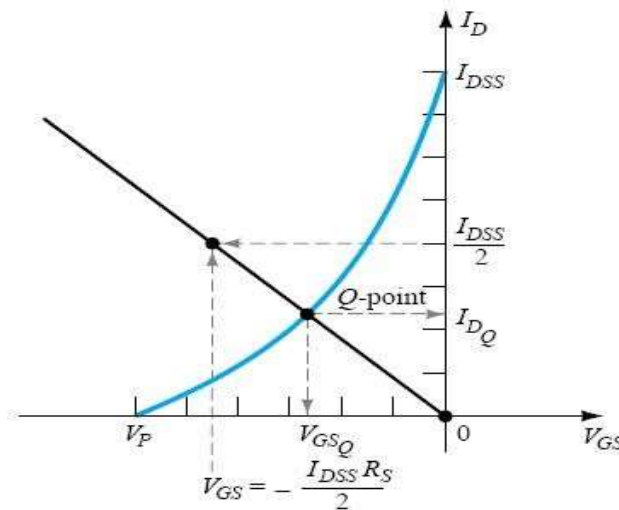
Fig 3.7 Sketching the self-bias line

The level of V_{DS} can be determined by applying Kirchhoff's voltage law to the output circuit, with the result that,
$V_{RS} + V_{DS} + V_{RD} - V_{DD} = 0$
Or, $\mathbf{V_{DS} = V_{DD} - I_D(R_S - R_D)}$ -----------------------------(3.11)

Keep in mind, $\mathbf{V_S = I_D R_S}$ --- (3.12)
$$\mathbf{V_G = 0V} \text{--} (3.13)$$
$$\mathbf{V_D = V_{DS} + V_S = V_{DD} - V_{RD}} \text{--------------------} (3.14)$$

<u>3.4</u>   VOLTAGE-DIVIDER BIASING

The voltage-divider bias arrangement applied to BJT transistor amplifiers is also applied to FET amplifiers as demonstrated by Fig. 3.8. The basic construction is exactly the same, but the dc analysis of each is quite different. $I_G = 0A$ for FET amplifiers, but the magnitude of I_B for common-emitter BJT amplifiers can affect the dc levels of current and voltage in both the input and output circuits. Recall that I_B provided the link between input and output circuits for the BJT voltage-divider configuration while V_{GS} will do the same for the FET configuration.

The network of Fig. 3.8 is redrawn as shown in Fig. 3.9 for the dc analysis. Note that all the capacitors, including the bypass capacitor C_S, have been replaced by an "open-circuit" equivalent. In addition, the source V_{DD} was separated into two equivalent sources to permit a further separation of the input and output regions of the network.
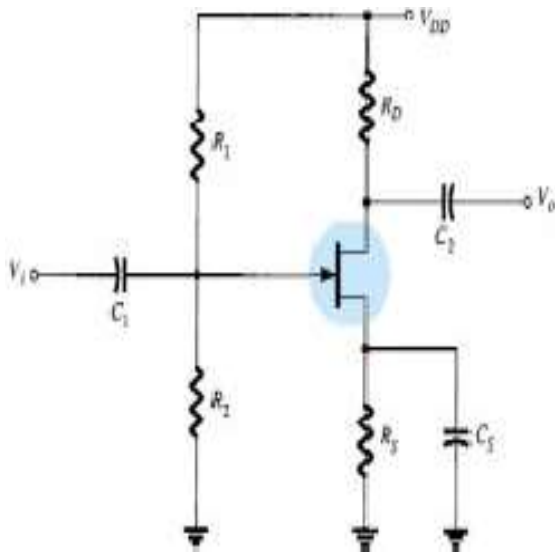
Fig 3.8 Voltage-divider bias arrangement   Fig 3.9 Redrawn network of
                                                          Fig.3.8 for dc analysis
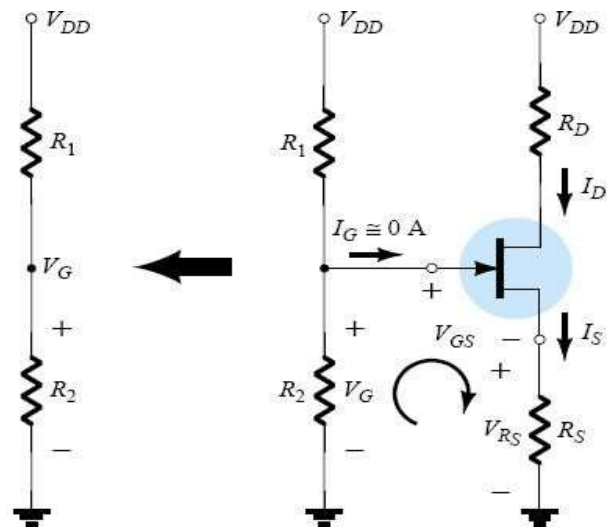
Since $I_G = 0A$, Kirchhoff's current law requires that $I_{R1} = I_{R2}$ and the series equivalent circuit appearing to the left of the figure can be used to find the level of V_G. The voltage V_G, equal to the voltage across R_2, can be found using the voltage-divider rule as follows:

$$V_G = V_{DD}R_2/R_1+R_2\text{-------------------------------- (3.15)}$$

Applying Kirchhoff's voltage law in the clockwise direction to the indicated loop of Fig. 3.9 will result in

$V_G - V_{GS} - V_{RS} = 0$

Substituting $V_{RS} = I_S R_S = I_D R_S$, we have

$$V_{GS} = V_G - I_D R_S \text{ ------------------------------------ (3.16)}$$

The result is an equation that continues to include the same two variables appearing in Shockley's equation: V_{GS} and I_D. The quantities V_G and R_S are fixed by the network construction. Equation (3.16) is still the equation for a straight line. The two points are:

$$V_{GS} = V_G|I_D = 0mA\text{---------------------------- (3.17)}$$
$$I_D = V_G/R_S|V_{GS} = 0V \text{ ------------------------(3.18)}$$
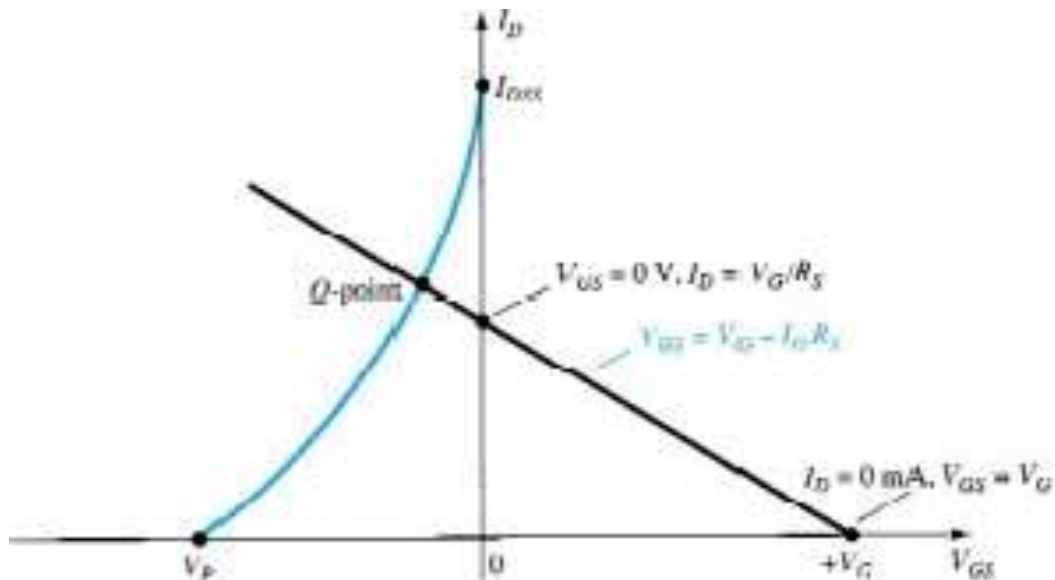
Fig 3.10 Sketching the network equation for the voltage-divider configuration

Increasing values of R_S result in lower quiescent values of I_D and more negative values of V_{GS}.

Once the quiescent values of I_{DQ} and V_{GSQ} are determined, the remaining network analysis can be performed in the usual manner. That is,

$$V_{DS} = V_{DD} - I_D(R_D + R_S) \text{ ----------------------(3.19)}$$
$$V_D = V_{DD} - I_D R_D \text{ -------------------------------- (3.20)}$$
$$V_S = I_D R_S \text{ --- (3.21)}$$
$$I_{R1} = I_{R2} = V_{DD}/R_1+R_2 \text{ ------------------------ (3.22)}$$

3.5   DEPLETION-TYPE MOSFETs

The similarities in appearance between the transfer curves of JFETs and depletion-type MOSFETs permit a similar analysis of each in the dc domain. The *primary difference* between the two is the fact that depletion-type MOSFETs permit operating points with positive values of V_{GS} and levels of I_D that exceeds I_{DSS}. In fact, for all the configurations discussed thus far, the analysis is the same if the JFET is replaced by a depletion-type MOSFET.
The only undefined part of the analysis is how to plot Shockley's equation for positive values of V_{GS}. How far into the region of positive values of V_{GS} and values of I_D greater than I_{DSS} does the transfer curve have to extend? For most situations, this required range will be fairly well defined by the MOSFET parameters and the resulting bias line of the network.

3.6   ENHANCEMENT-TYPE MOSFETs

The transfer characteristics of the enhancement-type MOSFET are quite different from those encountered for the JFET and depletion-type MOSFETs, resulting in a graphical solution quite different. First and foremost, recall that for the *n*-channel enhancement-type MOSFET, the drain current is zero for levels of gate-to-source voltage less than the threshold level $V_{GS(Th)}$, as shown in Fig. 3.11.
For levels of V_{GS} greater than $V_{GS(Th)}$, the drain current is defined by
$$\mathbf{I_D = k[V_{GS} - V_{GS(Th)}]^2} \text{----------------------} \quad (3.23)$$
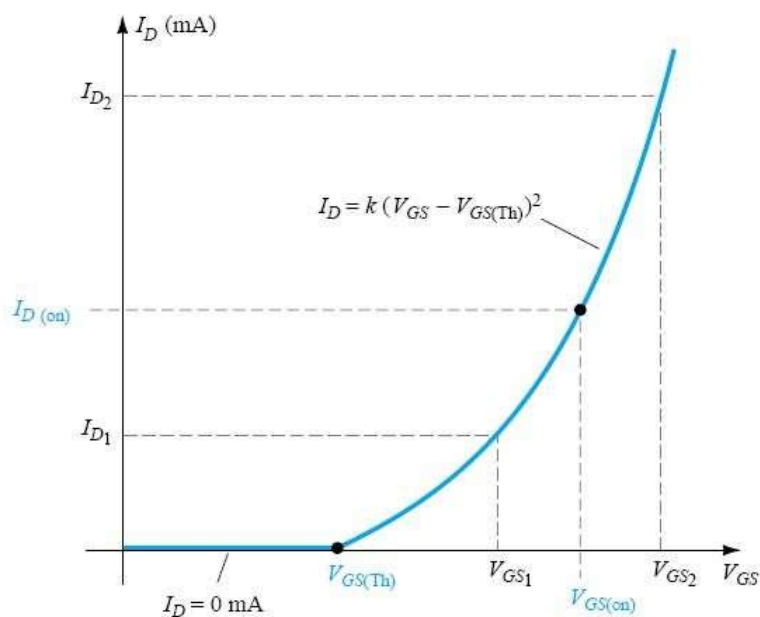
Fig 3.11 Transfer characteristics of an *n*-channel enhancement-type MOSFET

Since specification sheets typically provide the threshold voltage and a level of drain current (I_D(on)) and its corresponding level of V_{GS}(on), two points are defined immediately as shown in Fig. 3.11. To complete the curve, the constant k of Eq. (3.11) must be determined from the specification sheet data by substituting into Eq. (3.11) and solving for k as follows:

$$I_D = k[V_{GS} - V_{GS(Th)}]^2$$

Or, $I_{D(ON)} = k[V_{GS(ON)} - V_{GS(Th)}]^2$

$$k = I_{D(ON)} / [V_{GS(ON)} - V_{GS(Th)}]^2 \quad \text{-------------------} \quad (3.24)$$

Once k is defined, other levels of I_D can be determined for chosen values of V_{GS}. Typically, a point between $V_{GS(Th)}$ and $V_{GS(on)}$ and one just greater than $V_{GS(on)}$ will provide a sufficient number of points to plot Eq. (3.11).

<center>FEEDBACK BIASING ARRANGEMENT</center>

A popular biasing arrangement for enhancement-type MOSFETs is provided in Fig. 3.12. The resistor R_G brings a suitably large voltage to the gate to drive the MOSFET "on." Since $I_G = 0$ mA and $V_{RG} = 0$ V, the dc equivalent network appears as shown in Fig. 3.13.
A direct connection now exists between drain and gate, resulting in
$$V_D = V_G$$
and $\mathbf{V_{DS} = V_{GS}}$-------------------------- (3.25)
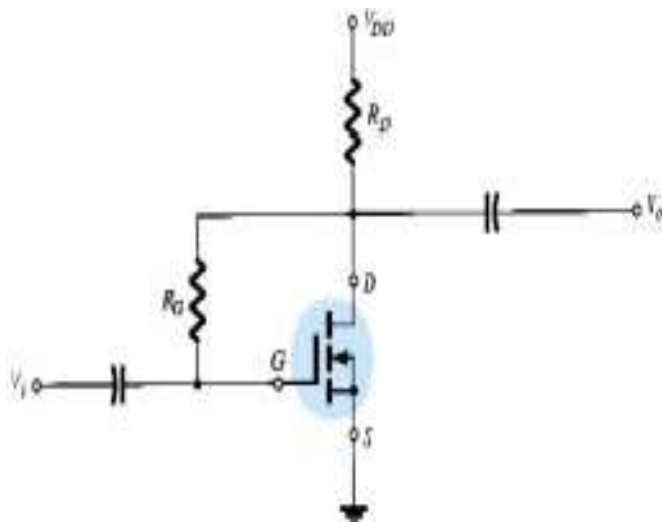
Fig 3.12 Feedback biasing arrangement   Fig 3.13 DC equivalent of
                                                                the network of Fig. 3.12
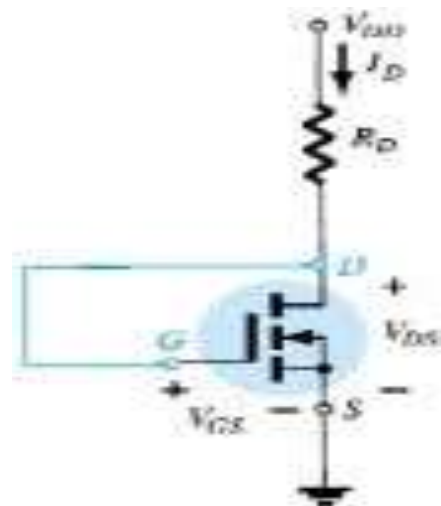
For the output circuit,

$V_{DS} = V_{DD} - I_D R_D$

$$\mathbf{V_{GS} = V_{DD} - I_D R_D} \text{-------------------------------------}(3.26)$$

The two points defining the Eq. (3.26) as a straight line,

$$\mathbf{V_{GS} = V_{DD}|I_{D=0mA}} \text{ ----------------------------} (3.27)$$
$$\mathbf{I_D = V_{DD}/R_D|V_{GS=0V}} \text{ -------------------------}(3.28)$$

The plots defined by Eqs. (3.23) and (3.26) appear in Fig. 6.38 with the resulting operating point.
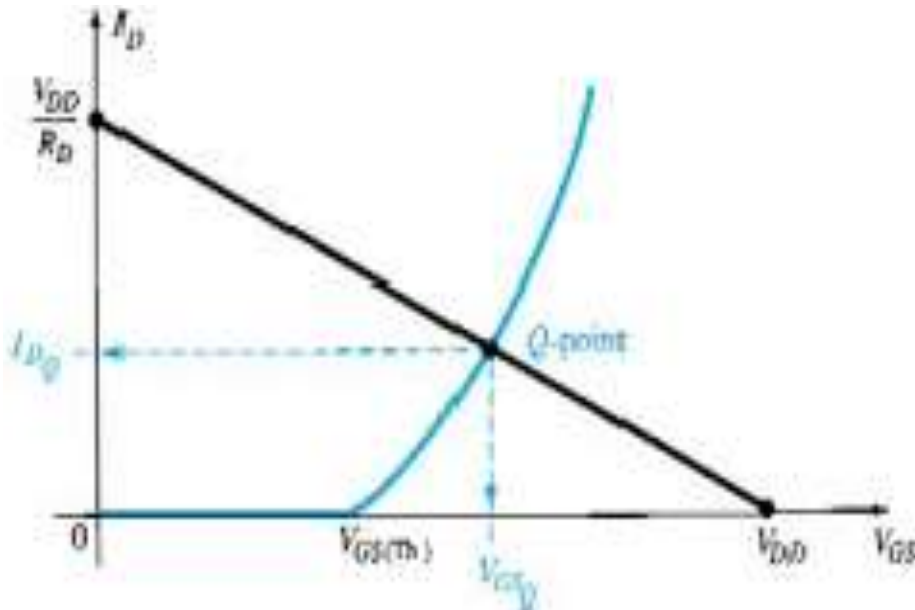
Fig 3.14 Determining the *Q*-point for the network of Fig. 3.12

VOLTAGE-DIVIDER BIASING ARRANGEMENT

A second popular biasing arrangement for the enhancement-type MOSFET appears in Fig. 3.15.

The fact that $I_G = 0$ mA results in the following equation for V_{GG} as derived from an application of the voltage-divider rule:

$$\mathbf{V_G = V_{DD}R_2/R_1 + R_2} \text{----------------------------} (3.29)$$

Applying Kirchhoff's voltage law around the indicated loop of Fig. 3.15 will result in,

$+V_G - V_{GS} - V_{RS} = 0$

$$\text{Or, } \mathbf{V_{GS} = V_G - I_D R_S} \text{ --------------------------} (3.30)$$
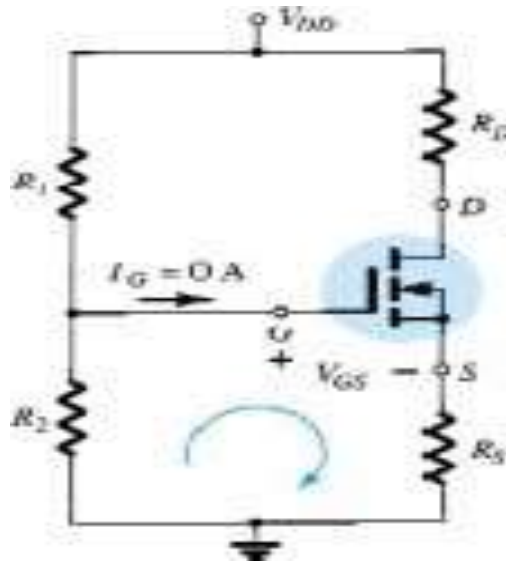
Fig 3.15 Voltage-divider biasing arrangement for an
n-channel enhancement MOSFET

For the output section:
$V_{RS} + V_{DS} + V_{RD} - V_{DD} = 0$
$$\text{Or, } \mathbf{V_{DS} = V_{DD} - I_D(R_S + R_D)} \text{ ------------------------- (3.31)}$$

Since the characteristics are a plot of I_D versus V_{GS} and Eq. (3.30) relates the same two variables, the two curves can be plotted on the same graph and a solution determined at their intersection. Once I_{DQ} and V_{GSQ} are known, all the remaining quantities of the network such as V_{DS}, V_D, and V_S can be determined.

Chapter 4 SMALL SIGNAL ANALYSIS OF BJTS

4.1   INTRODUCTION

A model is the combination of circuit elements, properly chosen, that best approximates the actual behavior of a semiconductor device under specific operating conditions.

Once the ac equivalent circuit has been determined, the graphical symbol of the device can be replaced in the schematic by this circuit and the basic methods of accircuit analysis (mesh analysis, nodal analysis, and Thévenin's theorem) can be applied to determine the response of the circuit.

There are two models commonly used in the small-signal ac analysis of transistor networks: the r_e model and the hybrid equivalent model.

4.2 AC EQUIVALENT-CIRCUIT MODEL
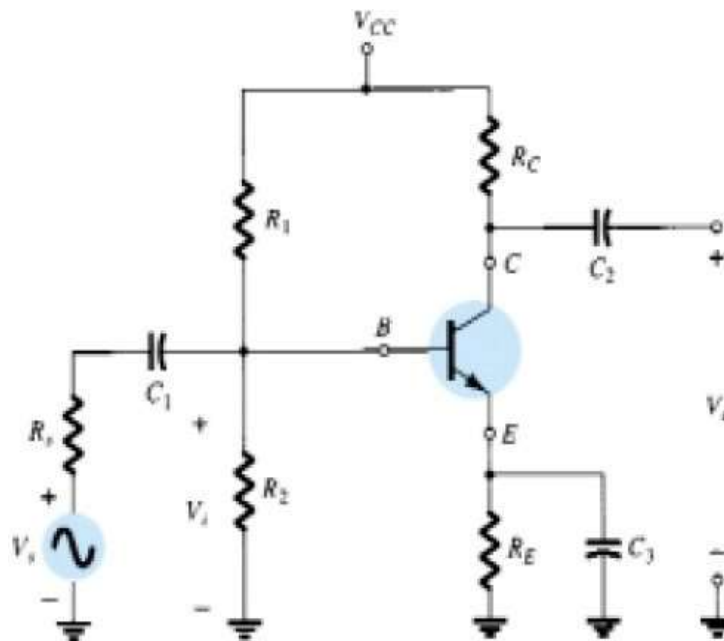
Fig 4.1 Transistor circuit
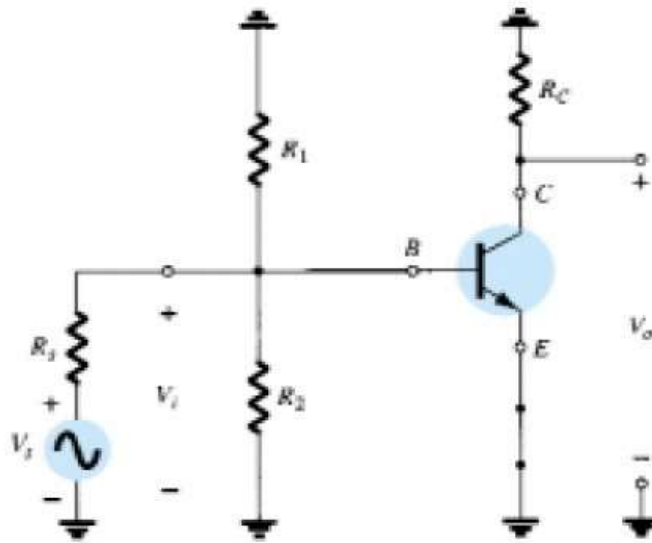
Fig 4.2 The network of Fig. 4.1 following removal of the dc supply and insertion of the short-circuit equivalent for the capacitors
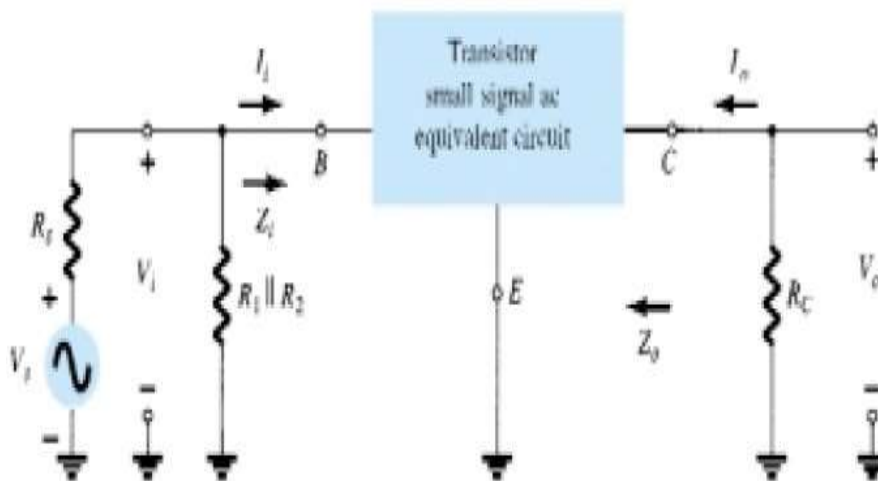
Fig 4.3 Circuit of Fig. 4.1 redrawn for small-signal ac analysis

In summary, the ac equivalent of a network is obtained by:

1. Setting all dc sources to zero and replacing them by a short-circuit equivalent
2. Replacing all capacitors by a short-circuit equivalent
3. Removing all elements bypassed by the short-circuit equivalents introduced by steps 1 and 2
4. Redrawing the network in a more convenient and logical form

<u>4.3 THE IMPORTANT PARAMETERS: Z_i, Z_0, A_v, A_i</u>

For the two-port (two pairs of terminals) system of Fig. 4.4, the input side (the side to which the signal is normally applied) is to the left and the output side (where the load is connected) is to the right.
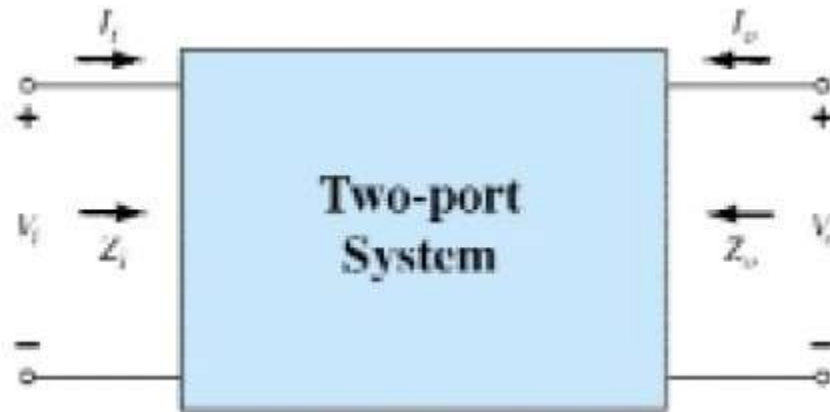
Fig 4.4 Two-port system

<u>Input Impedance, Z_i</u>

$Zi=V_i/Ii$

<u>Output Impedance, Z_o</u>

$Z_0=V_0/I_0$

<u>Voltage Gain, A_v</u>

$A_v =V_0/V_i$

<u>Current Gain, A_i</u>

$A_i =I_0/I_i$

4.4   THE *re* TRANSISTOR MODEL

The *re* model employs a diode and controlled current source to duplicate the behaviour of a transistor in the region of interest.

Common Base Configuration
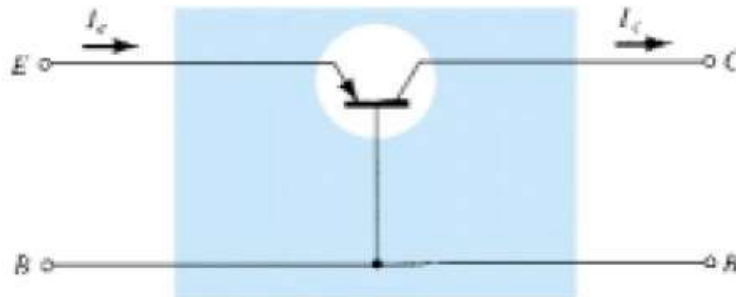
Fig 4.5 Common-base BJT transistor
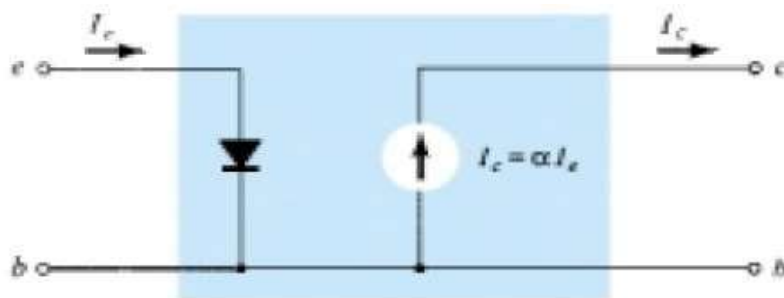
Fig 4.6 *re* model for the configuration

$$r_e = 26mV/I_E$$

The subscript *e* of *re* was chosen to emphasize that it is the dc level of emitter current that determines the ac level of the resistance of the diode of Fig. 4.6. Substituting the resulting value of *re* in Fig. 4.6 will result in the very useful model of Fig. 4.7.
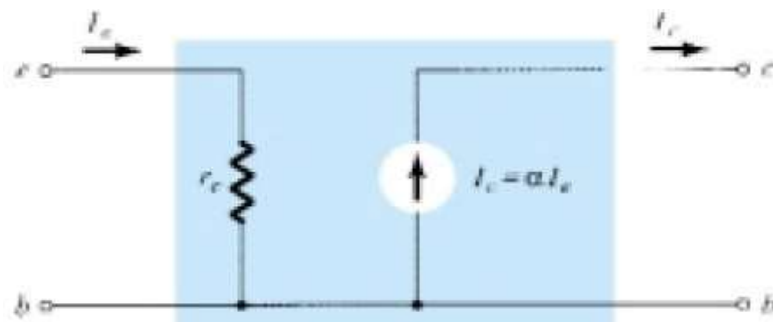
Fig. 4.7 Common Base r_e equivalent circuit

$$Z_i = r_e$$

$$Z_o = \infty \text{ ohm}$$

$$A_v = \alpha R_L/r_e = R_L/r_e$$

$$A_i = -\alpha = -1$$

Common Emitter Configuration
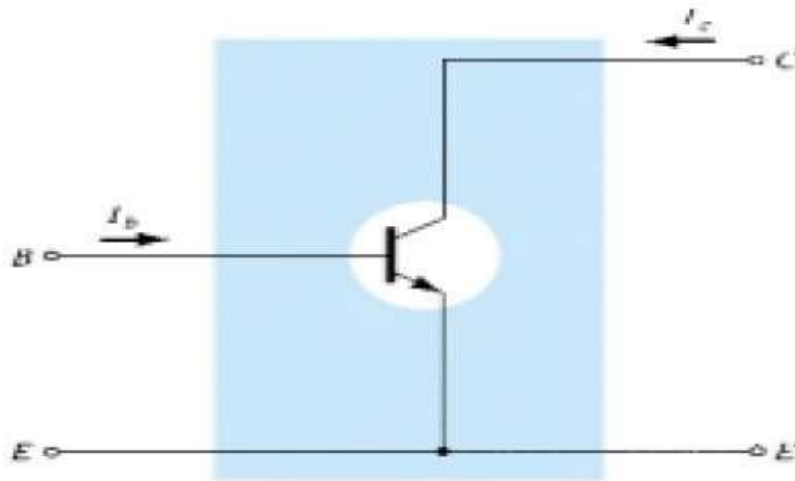
Fig 4.8 Common-emitter BJT transistor
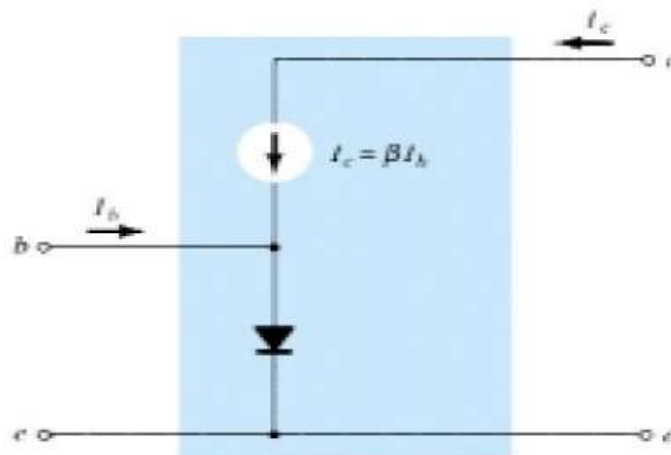
Fig 4.9 *re* model for the configuration
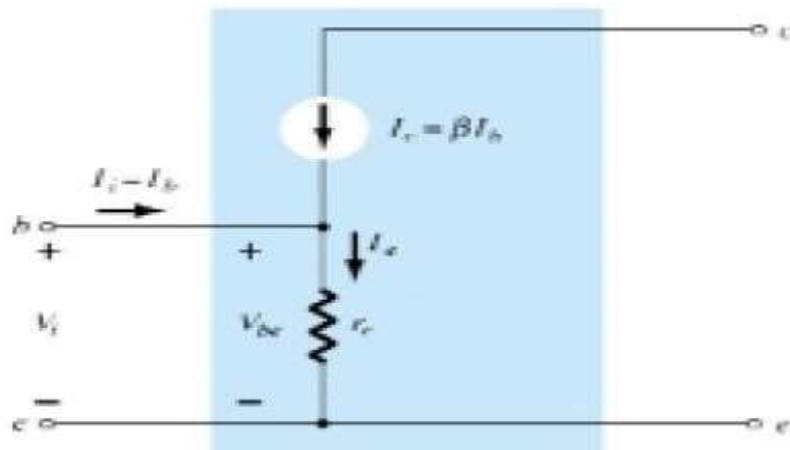
Fig 4.10 Common Emitter re equivalent circuit

$$Z_i = \beta R_E$$

$$Z_o = r_o$$

$$A_v = -R_L/r_e$$

$$A_i = \beta$$

4.5   THE HYBRID EQUIVALENT MODEL

The *re* model for a transistor is sensitive to the dc level of operation of the amplifier. The result is an input resistance that will vary with the dc operating point.

For the hybrid equivalent model, the parameters are defined at an operating point that may or may not reflect the actual operating conditions of the amplifier. This is due to the fact that specification sheets cannot provide parameters for an equivalent circuit at every possible operating point. They must choose operating conditions that they believe reflect the general characteristics of the device.

The quantities *hie*, *hre*, *hfe*, and *hoe* are called the *hybrid parameters* and are the components of a small-signal equivalent circuit.
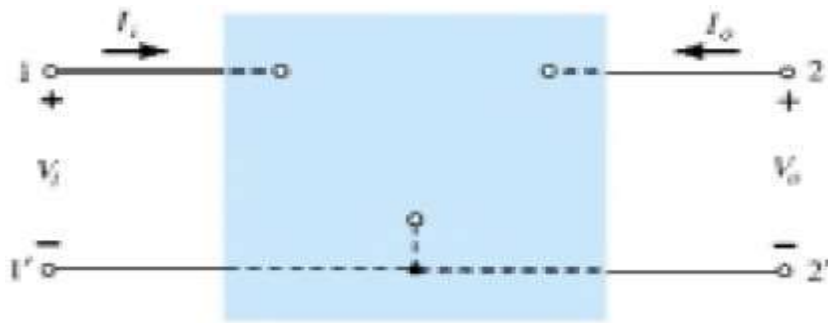
Fig 4.11 Two Port System

$V_i = h_{11}I_i + h_{12}V_o$
$I_o = h_{21}I_i + h_{22}V_o$

The parameters relating the four variables are called *h-parameters* from the word "hybrid." The term *hybrid* was chosen because the mixture of variables (*V* and *I*) in each equation results in a "hybrid" set of units of measurement for the *h*-parameters.

$\mathbf{h_{11}} = V_i/I_i|_{Vo=0} =$ **short-circuit input-impedance parameter**

$\mathbf{h_{12}} = V_i/V_o|_{Ii=0} =$ **open-circuit reverse transfer voltage ratio parameter**

$\mathbf{h_{21}} = I_o/I_i|_{Vo=0} =$ **short-circuit forward transfer current ratio parameter**

$\mathbf{h_{22}} = I_o/V_o|_{Io=0} =$ **open-circuit output admittance parameter**
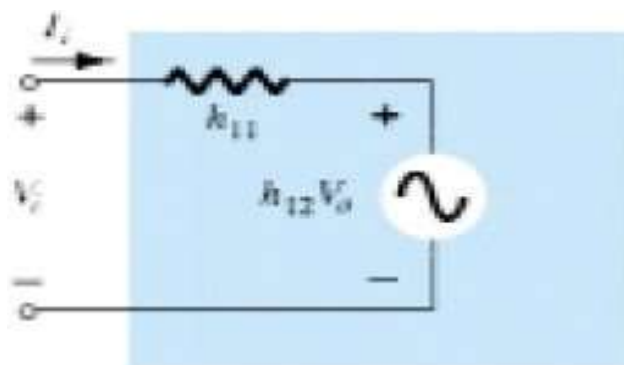
Fig 4.12 Hybrid Input equivalent circuit
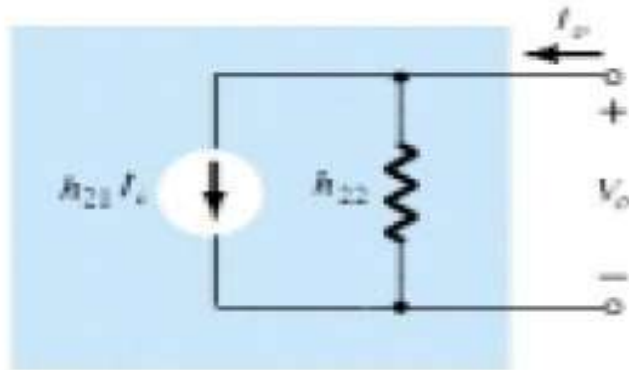
Fig 4.13 Hybrid Output equivalent circuit
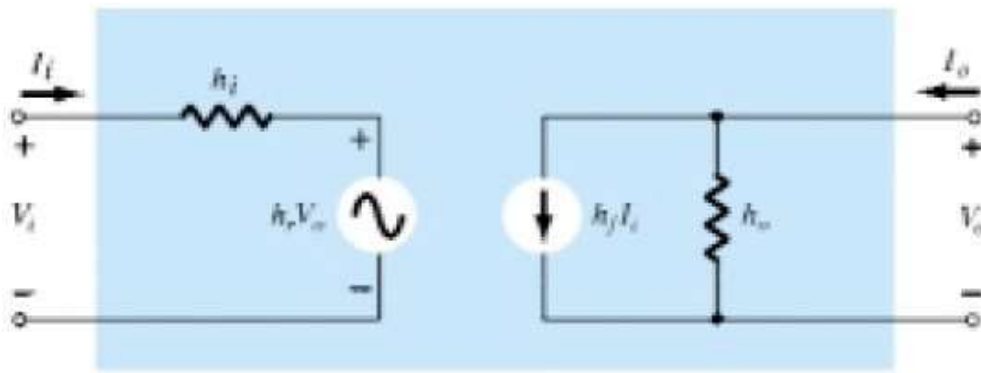
Fig 4.14 Complete Hybrid Equivalent Model

Where,

h_{11} = input resistance = h_i
h_{12} = reverse transfer voltage ratio = h_r
h_{21} = forward transfer current ratio = h_f
h_{22} = output conductance = h_o

Common Base Configuration
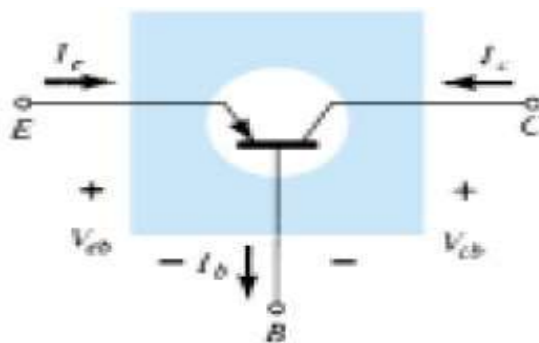
Fig 4.15 Graphical Symbol
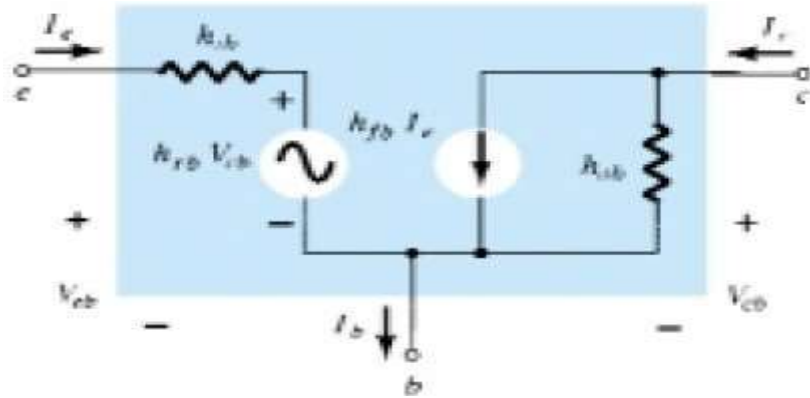
Fig 4.16 Hybrid equivalent circuit

<u>Common Emitter Configuration</u>
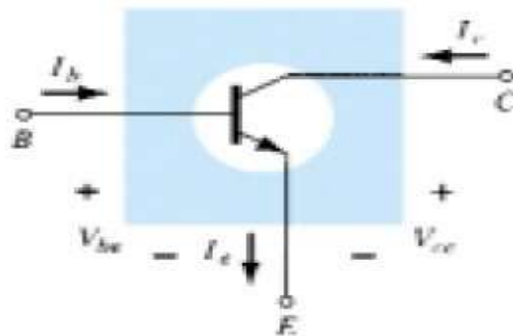
Fig 4.17 Graphical Symbol
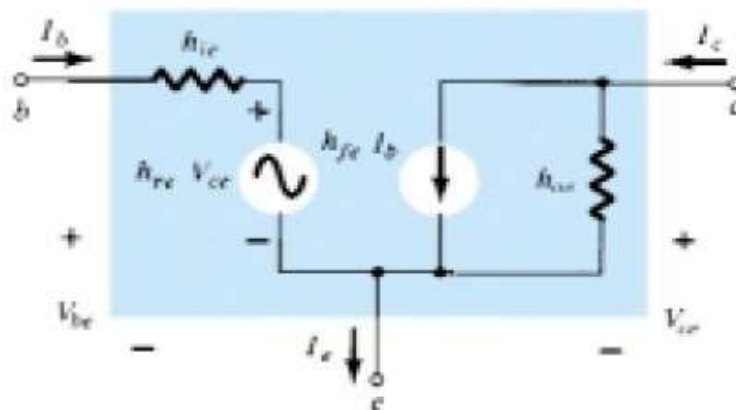
Fig 4.18 Hybrid equivalent model

Common Emitter (Hybrid vs r_e model)
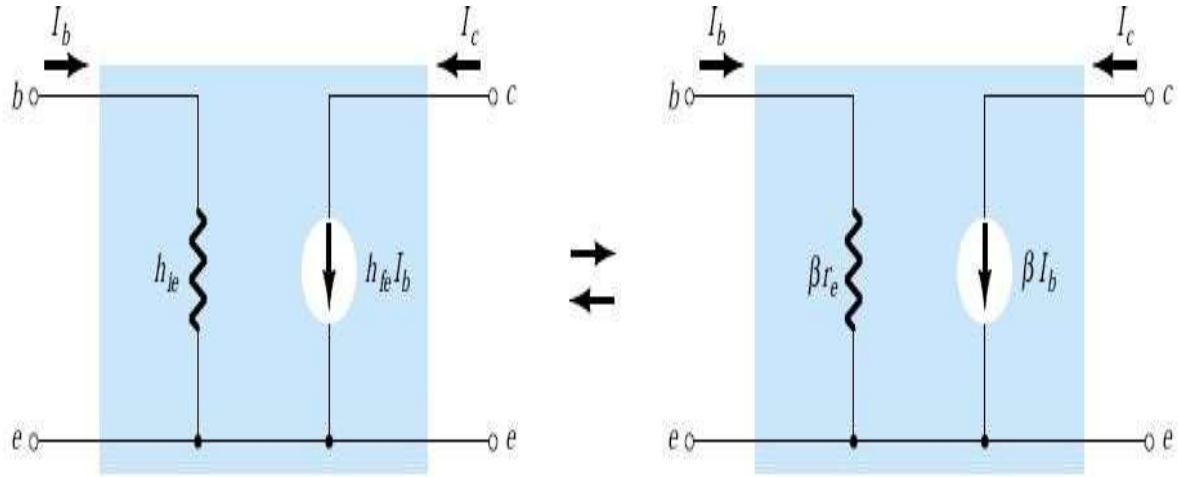
$$\mathbf{h_{ie} = \beta_{re}}$$

$$\mathbf{h_{fe} = \beta_{ac}}$$

Common Base (Hybrid vs r_e model)
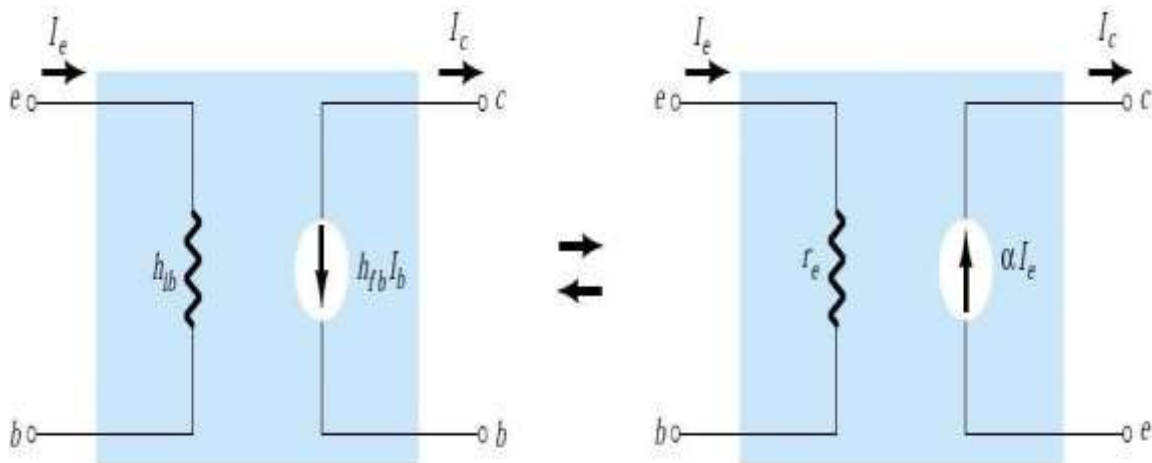
$$\mathbf{h_{ib} = r_e}$$

$$\mathbf{h_{fb} = -\alpha = -1}$$

4.6 GRAPHICAL DETERMINATION OF THE *h*-PARAMETERS

Using partial derivatives (calculus), it can be shown that the magnitude of the *h*-parameters for the small-signal transistor equivalent circuit in the region of operation.

For the common-emitter configuration h-parameters can be found using the following equations:

$\mathbf{h_{ie}} = \partial \mathbf{v_i}/\partial \mathbf{i_i} = \partial \mathbf{v_{be}}/\partial \mathbf{i_b} = \Delta \mathbf{v_{be}}/\Delta \mathbf{i_b}|_{\mathbf{VCE=constant}}$ **(ohms)**

$\mathbf{h_{re}} = \partial \mathbf{v_i}/\partial \mathbf{v_o} = \partial \mathbf{v_{be}}/\partial \mathbf{v_{ce}} = \Delta \mathbf{v_{be}}/\Delta \mathbf{v_{ce}}|_{\mathbf{IB=constant}}$ **(unitless)**

$\mathbf{h_{fe}} = \partial \mathbf{i_o}/\partial \mathbf{i_i} = \partial \mathbf{i_c}/\partial \mathbf{i_b} = \Delta \mathbf{i_c}/\Delta \mathbf{i_b}|_{\mathbf{VCE=constant}}$ **(unitless)**

$\mathbf{h_{oe}} = \partial \mathbf{i_o}/\partial \mathbf{v_o} = \partial \mathbf{i_c}/\partial \mathbf{v_{ce}} = \Delta \mathbf{i_c}/\Delta \mathbf{v_{ce}}|_{\mathbf{IB=constant}}$ **(ohms)**
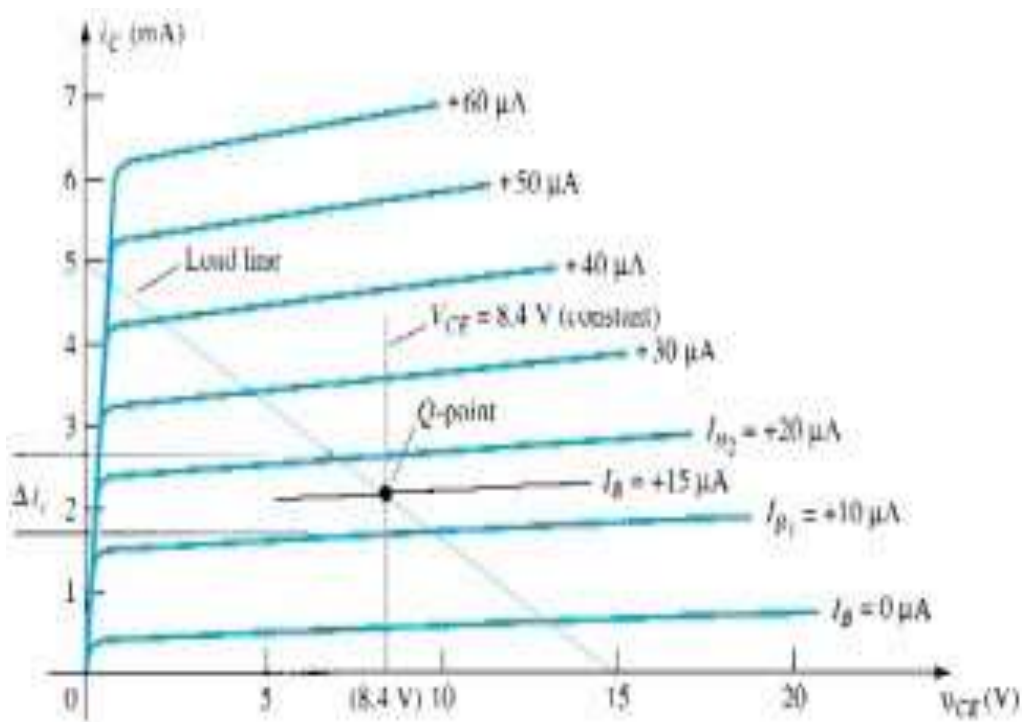
Fig 4.19 h_{fe} determination
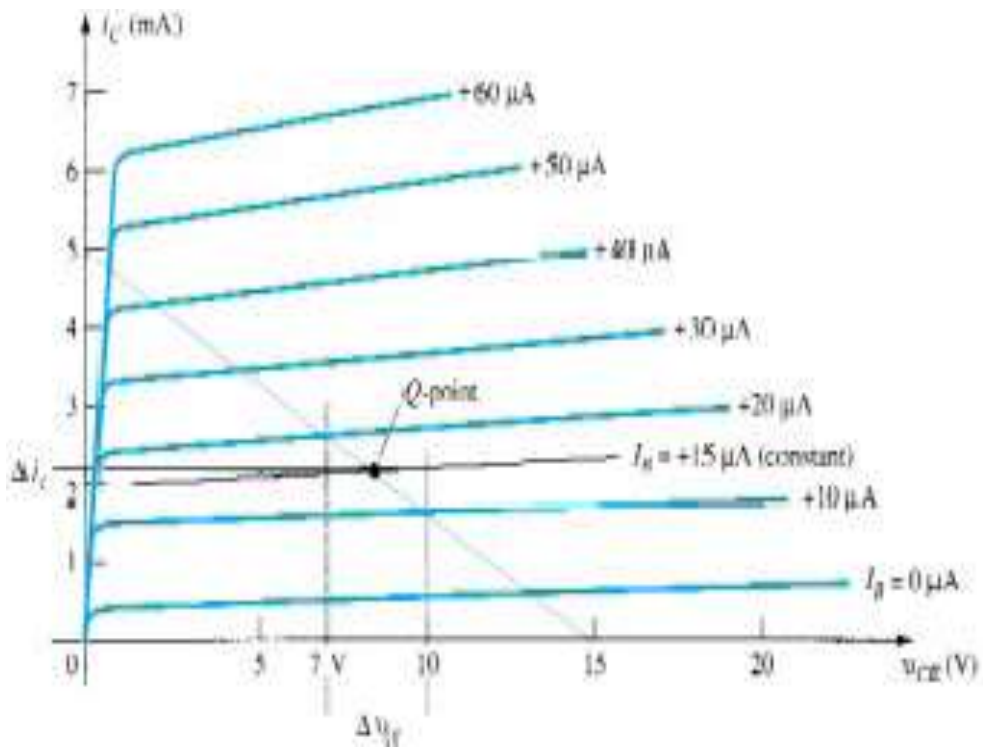
Fig 4.20 h_{oe} determination
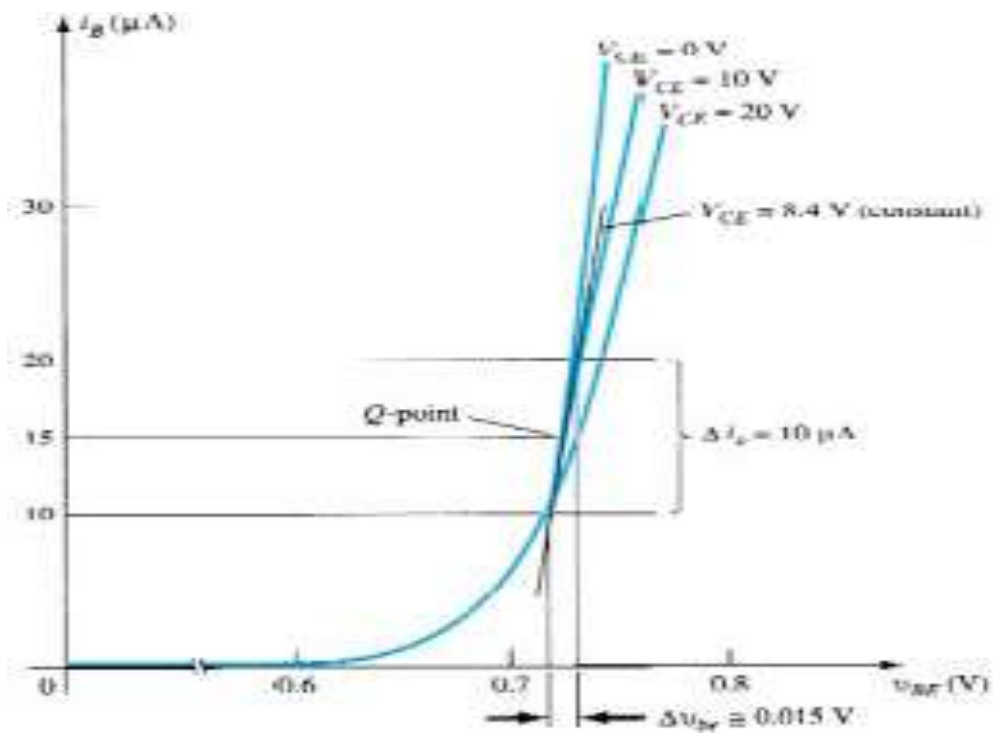
Fig 4.21 h_{ie} determination
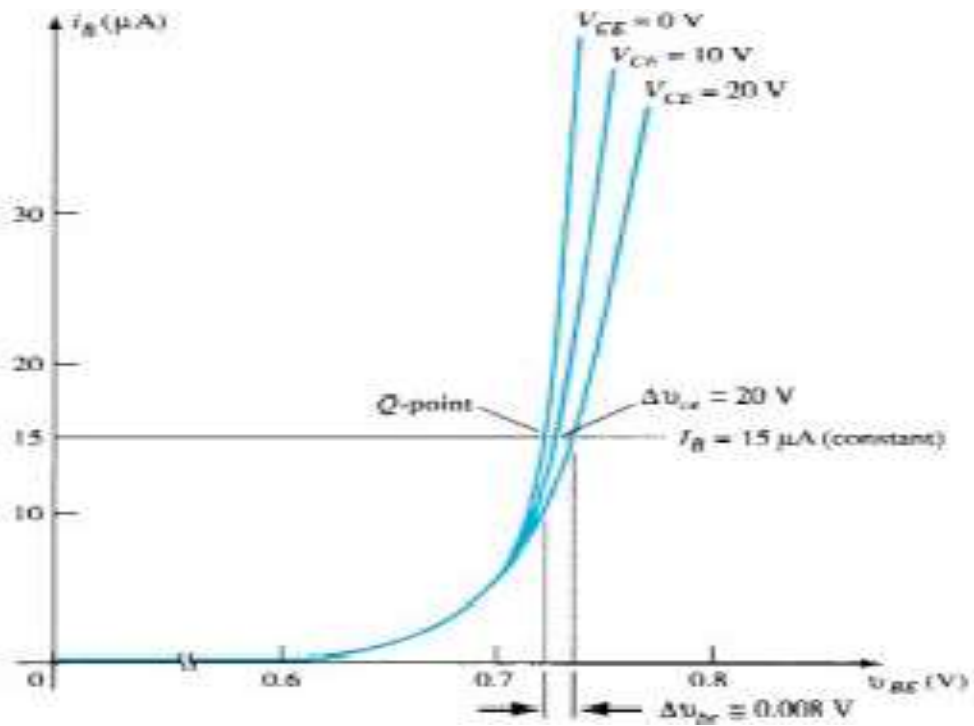
Fig 4.22 h_{re} determination
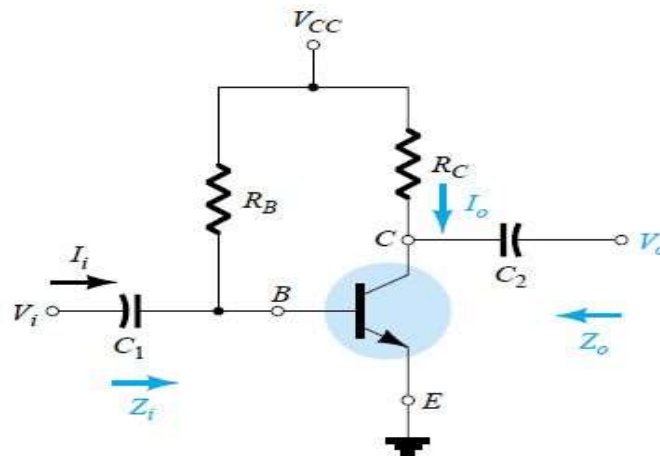
4.7 COMMON EMITTER FIXED-BIAS CONFIGURATION
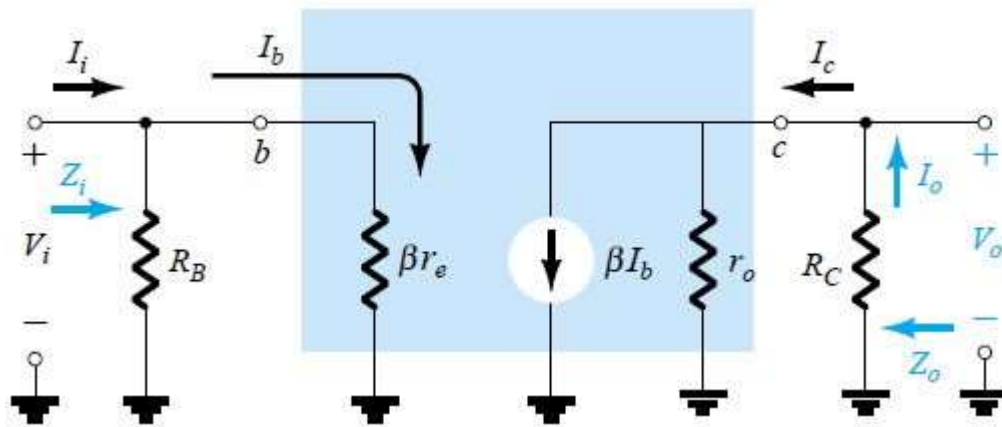

Fig. 4.23 Common-emitter fixed-bias configuration

Fig. 4.24 Substituting the *re* model into the network of Fig 4.23

$$\mathbf{Z_i} = R_B \| \beta r_e$$

$$Z_o = R_C \| r_o$$

$$A_v = -(r_o \| R_c)/r_e$$

$$A_i = (R_B \beta r_o)/((r_o + R_c)(R_B + \beta r_e))$$
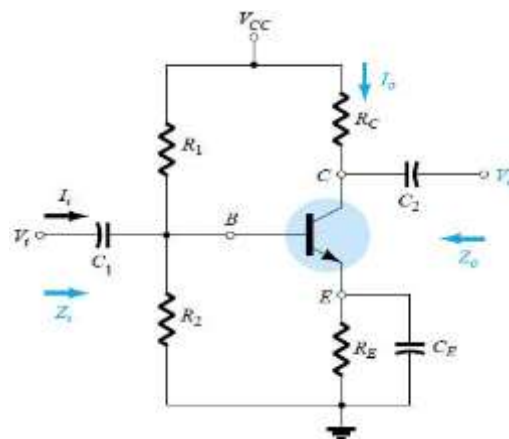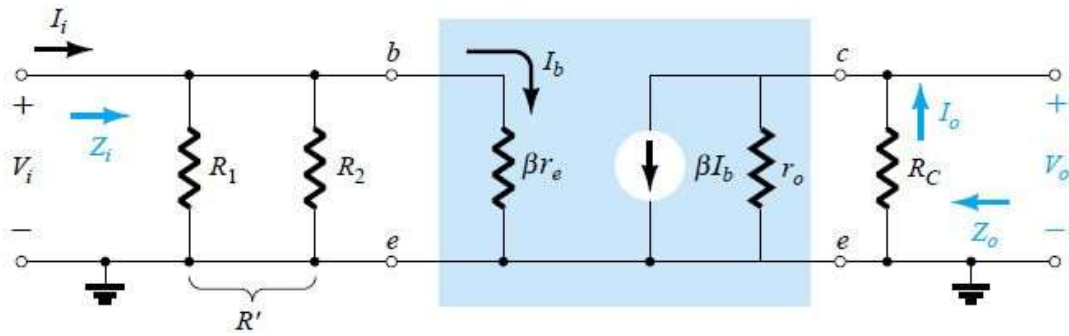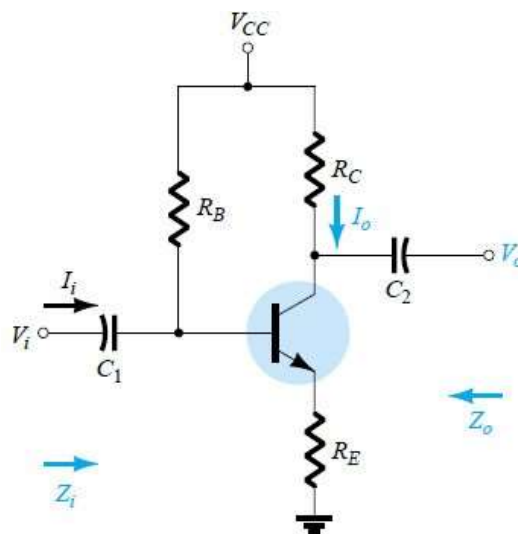
4.8 COMMON EMITTER VOLTAGE-DIVIDER BIAS CONFIGURATION

Fig. 4.24 Voltage – divider bias configuration

Fig. 4.25 Substituting the *re* model into the network of Fig 4.24

$$Z_i = R_1 \| R_2 \| \beta r_e$$

$$Z_o = r_o \| R_c$$

$$A_v = -(r_o \| R_c)/r_e$$

$$A_i = (R_B \beta r_o)/((r_o + R_c)(R_B + \beta r_e))$$

4.9   COMMON EMITTER-BIAS CONFIGURATION (UNBYPASSED)
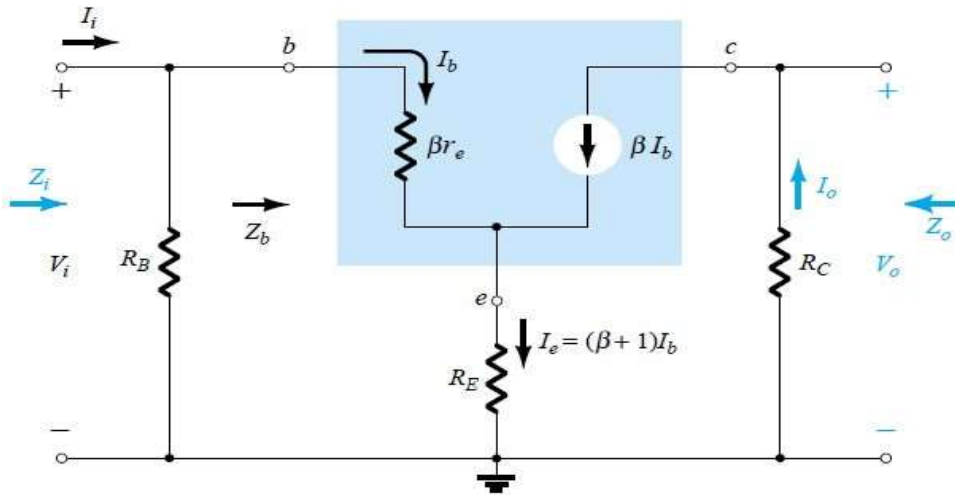

Fig. 4.27 Common Emitter Bias Configuration

Fig. 4.28 Substituting the *re* model into the network of Fig 4.27

$$Z_i = R_B \| \beta(r_e + R_E)$$

$$Z_o = R_c$$

$$A_v = -(R_c)/(r_e + R_E)$$

$$A_i = (R_B\beta)/(R_B + \beta(r_e + R_E))$$

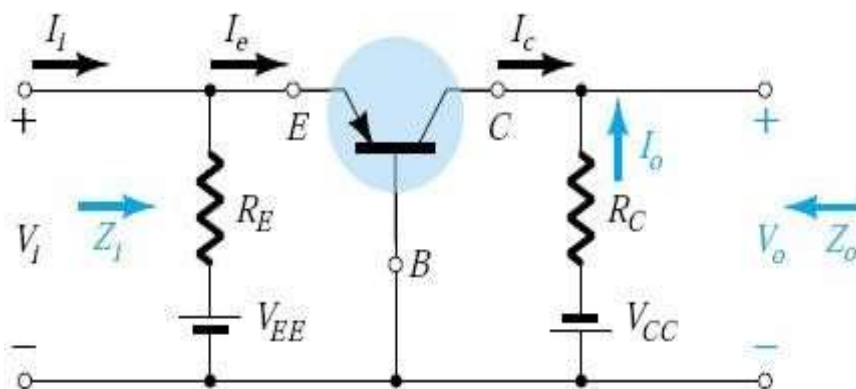4.10   COMMON BASE CONFIGURATION
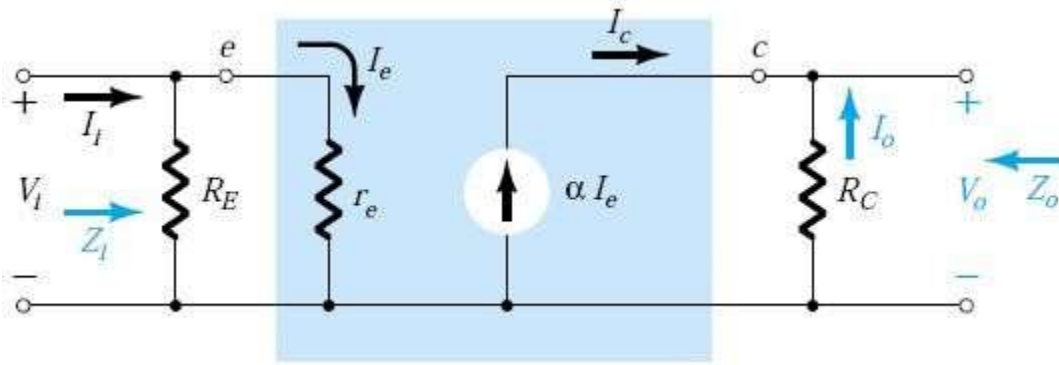

Fig. 4.29 Common Base Configuration

Fig. 4.30 Substituting the *re* model into the network of Fig 4.29

$$Z_i = R_E || r_e$$

$$Z_O = R_C$$

$$A_V = R_C / r_e$$

$$A_i = -1$$

4.11   COLLECTOR FEEDBACK CONFIGURATION

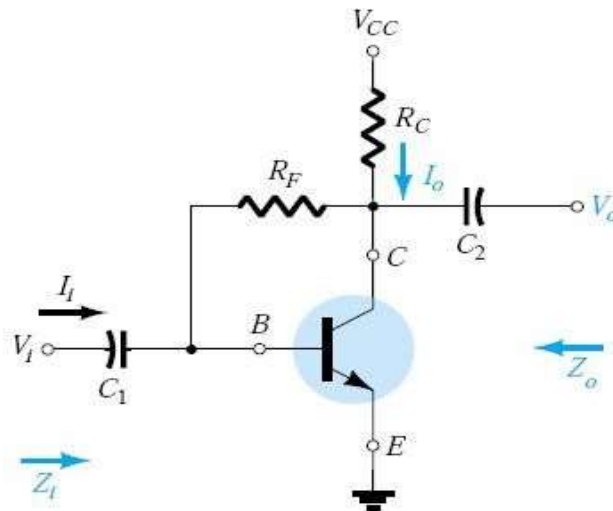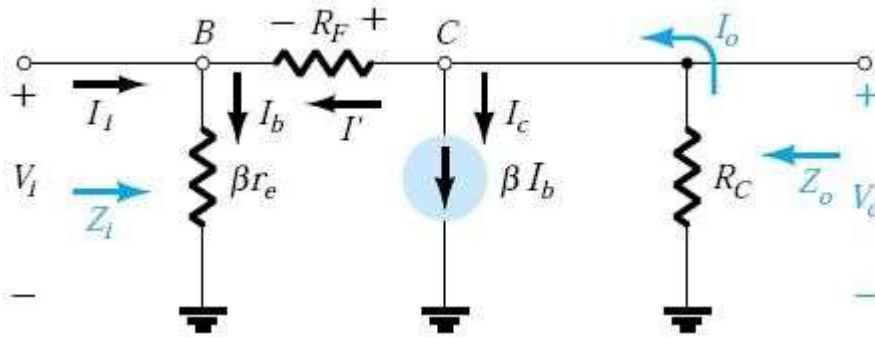

Fig. 4.31 Collector Feedback Configuration

Fig 4.32 Substituting the *re* model into the network of Fig 4.31

$$Z_i = r_e/(1/\beta+R_C/R_F)$$

$$Z_O = R_C \| R_F$$

$$A_V = -R_C/r_e$$

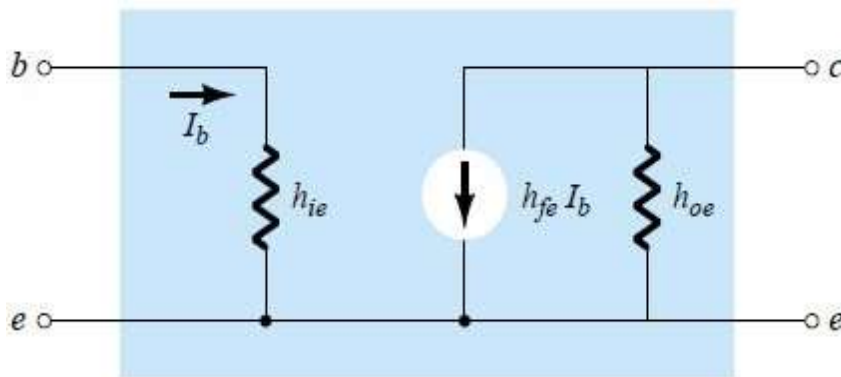$$A_i = R_F/R_C$$

4.12   APPROXIMATE HYBRID EQUIVALENTCIRCUIT

Fig. 4.33 Approximate Common-Emitter hybrid equivalent circuit
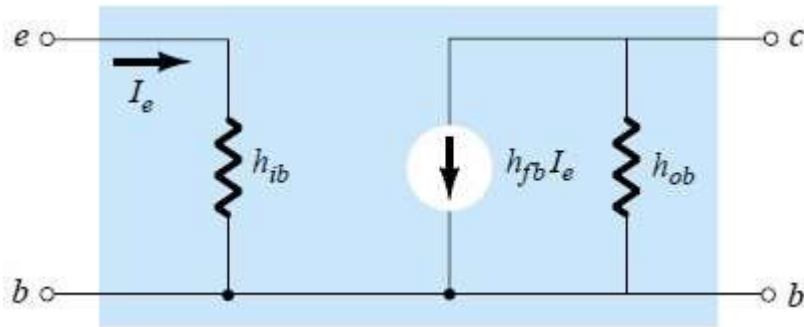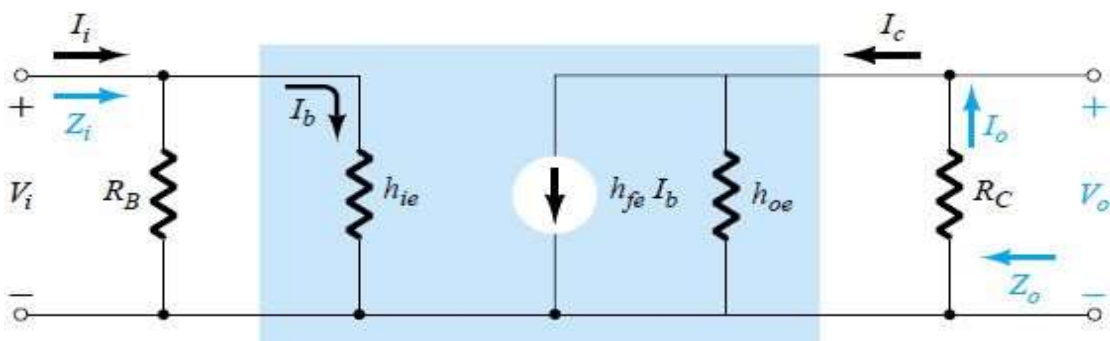
Fig. 4.34 Approximate Common-Base hybrid equivalent circuit

FIXED-BIAS CONFIGURATION
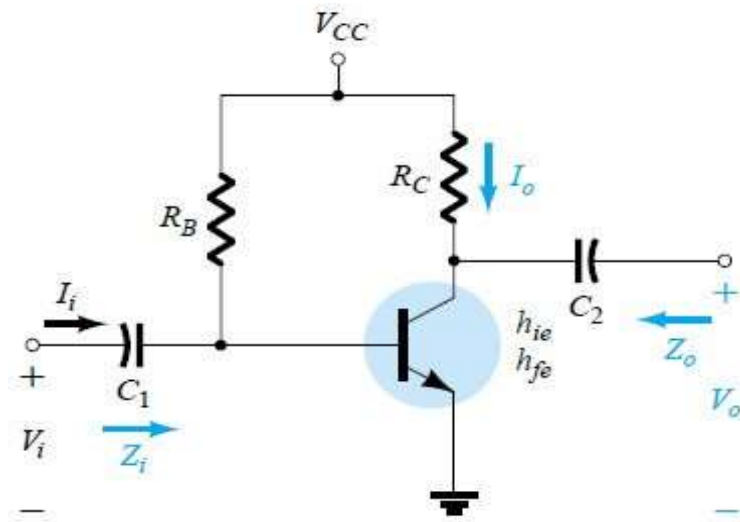
$$Z_i = R_B \| h_{ie}$$
$$Z_o = R_c \| (1/h_{ie})$$
$$A_v = -(h_{fe}(R_c \| (1/h_{oe})))/h_{ie}$$
$$A_i = h_{fe}$$

VOLTAGE-DIVIDER BIAS CONFIGURATION
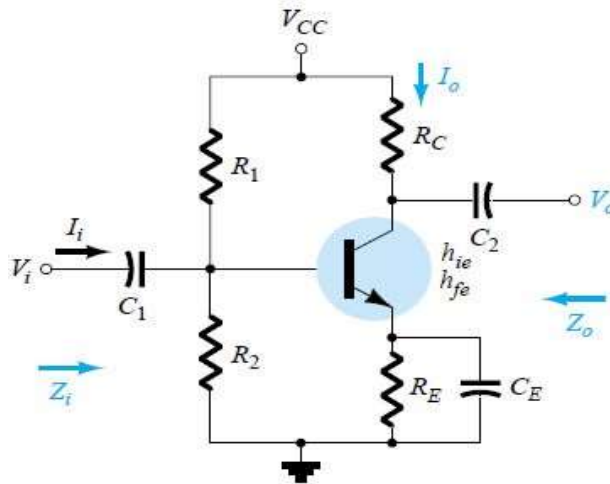
$$Z_i = R_B \| h_{ie}$$
$$Z_o = R_c \| (1/h_{ie})$$
$$A_v = -(h_{fe}(R_c \| (1/h_{oe})))/h_{ie}$$
$$A_i = h_{fe}$$

UNBYPASSED EMITTER-BIAS CONFIGURATION

$$Z_i = h_{ie} + h_{fe}R_E$$
$$Z_o = R_c$$
$$A_v = -(h_{fe}R_c)/(h_{ie} + R_E h_{fe})$$
$$A_i = (h_{fe}(R_B \| Z_b))/(h_{ie} + R_E h_{fe})$$

<u>4.14 CASCADED SYSTEMS</u>

The two-port systems approach is particularly useful for cascaded systems such as that appearing in Fig. 10.35, where Av1,Av2,Av3, and so 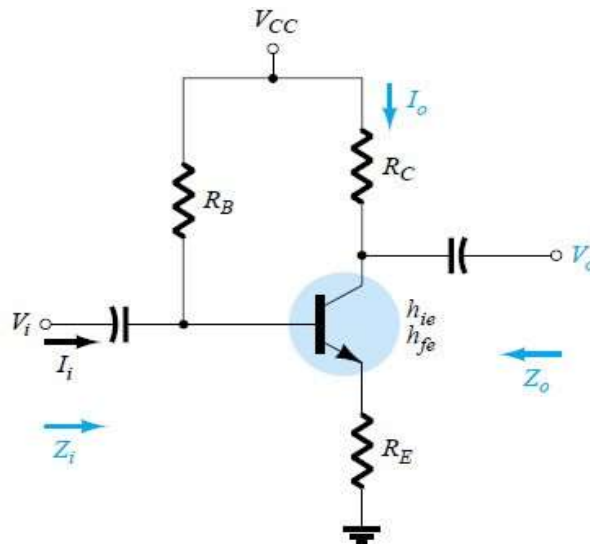on, are the voltage gains of each stage under loaded conditions. That is, Av1is determined with the input impedance to Av2 acting as the load on Av1. For Av2, Av1 will determine the signal strength and source impedance at the input to Av2.The total gain of the system is then determined by the product of the individual gains as follows:

$$A_{vt}=A_{v1} \cdot A_{v2} \cdot A_{v3} \cdot A_{v4}\ldots\ldots\ldots\ldots\ldots$$

and the total current gain by

$$A_{iT} = - A_{vT}(Z_{i1}/ R_L)$$

No matter how perfect the system design, the application of a load to a two-port

system will affect the voltage gain. Therefore, there is no possibility of a situation where Av1,Av2, and so on, of Fig. 10.35 are simply the no-load values. The loading of each succeeding stage must be considered.
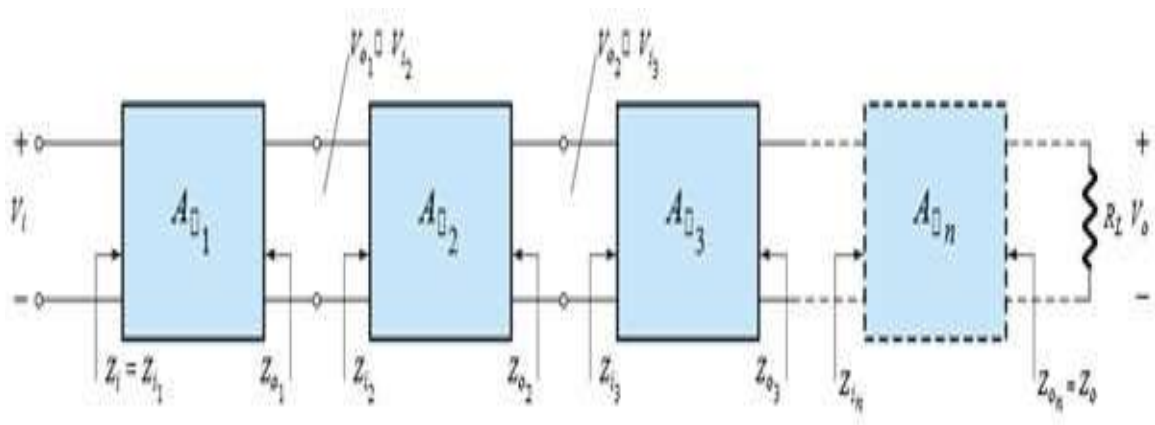

Fig. 4.35 Cascaded Systems

CHAPTER 5 SMALL SIGNAL ANALYSIS OF FETS

5.1   INTRODUCTION

Field-effect transistor amplifiers provide an excellent voltage gain with the added feature of a high input impedance. They are also considered low-power consumption configurations with good frequency range and minimal size and weight. Both JFET and depletion MOSFET devices can be used to design amplifiers having similar voltage gains. The depletion MOSFET circuit, however, has a much higher input impedance than a similar JFET configuration.

While a BJT device controls a large output (collector) current by means of a relatively small input (base) current, the FET device controls an output (drain) current by means of a small input (gate-voltage) voltage. In general, therefore, the BJT is a *current-controlled* device and the FET is a *voltage-controlled* device. In both cases, however, note that the output current is the controlled variable. Because of the high input characteristic of FETs, the ac equivalent model is somewhat simpler than that employed for BJTs. While the BJT had an amplification factor β (beta), the FET has a transconductance factor, *gm*.

The FET can be used as a linear amplifier or as a digital device in logic circuits. In fact, the enhancement MOSFET is quite popular in digital circuitry, especially in CMOS circuits that require very low power consumption. FET devices are also widely used in high-frequency applications and in buffering (interfacing) applications.

While the common-source configuration is the most popular providing an inverted, amplified signal, one also finds common-drain (source-follower) circuits providing unity gain with no inversion and common-gate circuits providing gain with no inversion. As with BJT amplifiers, the important circuit features described in this chapter include voltage gain, input impedance, and output impedance. Due to the very high input impedance, the input current is generally assumed to be 0 μA and the current gain is an undefined quantity. While the voltage gain of an FET amplifier is generally less than that obtained using a BJT amplifier, the FET amplifier provides much higher input impedance than that of a BJT configuration. Output impedance values are comparable for both BJT and FET circuits.

5.2   FET SMALL-SIGNAL MODEL

The ac analysis of an FET configuration requires that a small-signal ac model for the FET be developed. A major component of the ac model will reflect the

fact that an ac voltage applied to the input gate-to-source terminals will control the level of current from drain to source.

The gate-to-source voltage controls the drain-to-source (channel) current of an FET.

A dc gate-to-source voltage controlled the level of dc drain current through a relationship known as Shockley's equation: $I_D = I_{DSS}(V_{GS} - V_p)^2$

The *change* in collector current that will result from a *change* in gate-to-source voltage can be determined using the transconductance factor *gm* in the following manner: $\Delta I_D = g_m \Delta V_{GS}$

The prefix *trans-* in the terminology applied to *gm* reveals that it establishes a relationship between an output and input quantity. The root word *conductance* was chosen because *gm* is determined by a voltage-to-current ratio similar to the ratio that defines the conductance of a resistor $G = 1/R = I/V$ or, $g_m = \Delta I_D / \Delta V_{GS}$

5.3. GRAPHICAL DETERMINATION OF gm

$$g_m \equiv \frac{\Delta I_D}{\Delta V_{GS}} \ (= \text{Slope at } Q\text{-point})$$
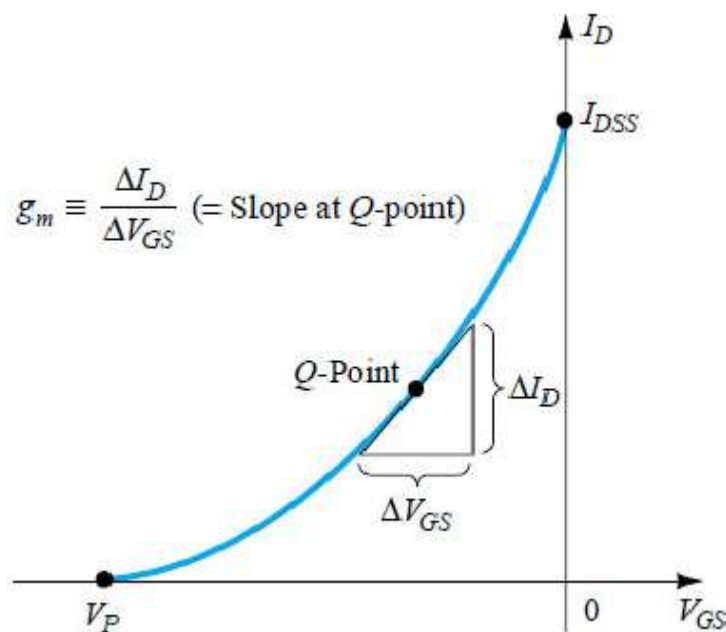
$g_m = m = \Delta y / \Delta x = \Delta I_D / \Delta V_{GS}$

5.4 MATHEMATICAL DEFINITION OF gm

$g_m = 2\, I_{DSS} / |V_p|\, [1 - V_{GS}/V_p]$

$gm0 = 2 I_{DSS}/|Vp|$

$gm = gm0[1 - V_{GS}/Vp]$

Impact of I_D on gm : $gm = gm0[1 - V_{GS}/Vp] = gm0(\sqrt{I_D/I_{DSS}})$

FET Input Impedance zi: $Zi(FET) = \infty\Omega$

FET Output Impedance zo: $Zo(FET) = rd$

5.4   FET AC EQUIVALENT CIRCUIT

a model for the FET transistor in the ac domain can be constructed. The control of *Id* by *Vgs* is included   as a current source *gmVgs* connected from drain to source as shown in Fig.   5.1. The current source has its arrow pointing from drain to source to establish a 180° phase shift between output and input voltages as will occur in actual operation.
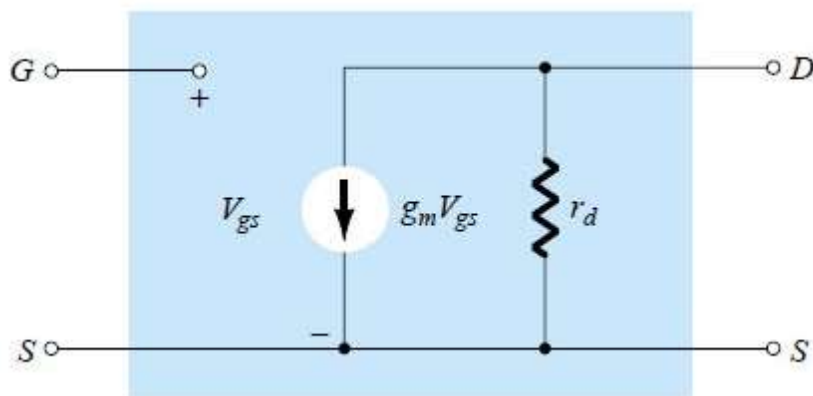

Fig. 5.1 FET AC Equivalent circuit

The input impedance is   represented by the open circuit at the   input terminals and the output impedance by the resistor *rd* from drain to source. Note that the gate to source voltage is now represented by *Vgs* (lower-case subscripts) to distinguish it from dc levels. In addition, take note of the fact that the source is common to both input and output circuits while the gate and drain terminals are only in "touch" through the controlled current source *gmVgs*.

In situations where *rd* is ignored (assumed sufficiently large to other elements of the network to be approximated by an open circuit), the equivalent circuit is

simply a current source whose magnitude is controlled by the signal *Vgs* and parameter *gm*— clearly a voltage-controlled device.

5.5 FIXED BIAS CIRCUIT
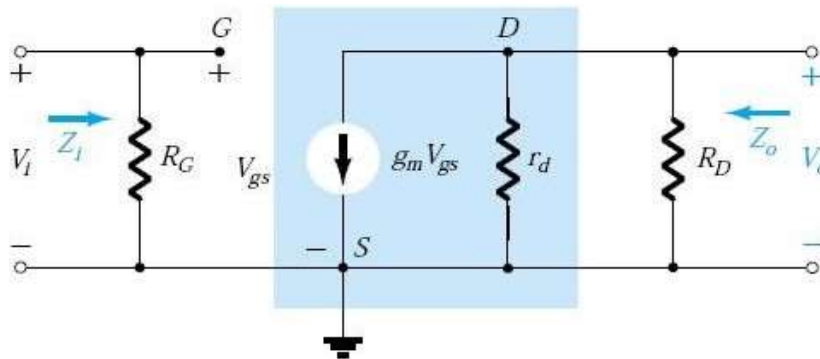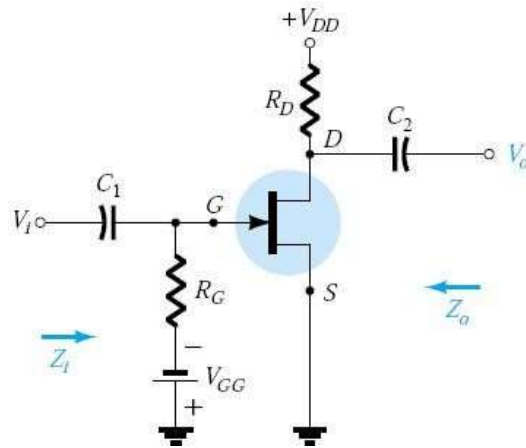
$$Z_i = R_G$$

$$Z_O = R_D \| r_d$$

$$Av = -gm(R_D \| r_d)$$

5.6   <u>SELF BIAS CIRCUIT (Unbypassed Rs)</u>
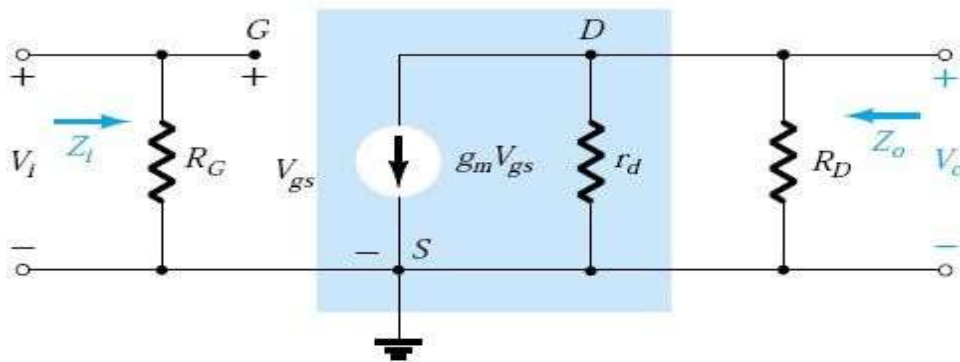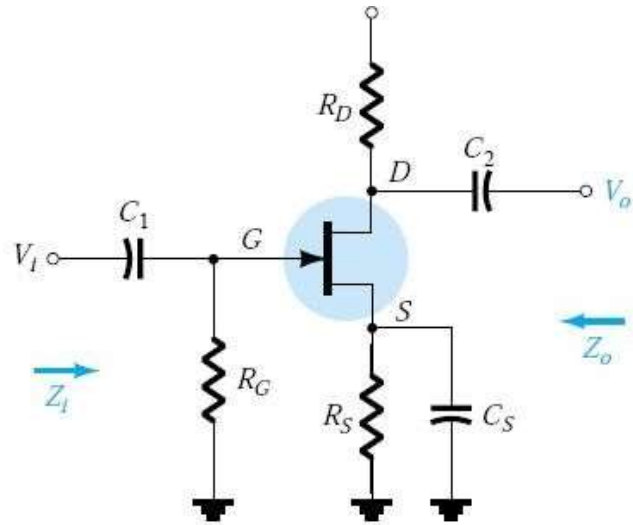
$$Z_i = R_G$$

$$Z_o = R_D \| r_d$$

$$A_v = -g_m(R_D \| r_d)$$

5.6 SELF BIAS CIRCUIT (Bypassed Rs)
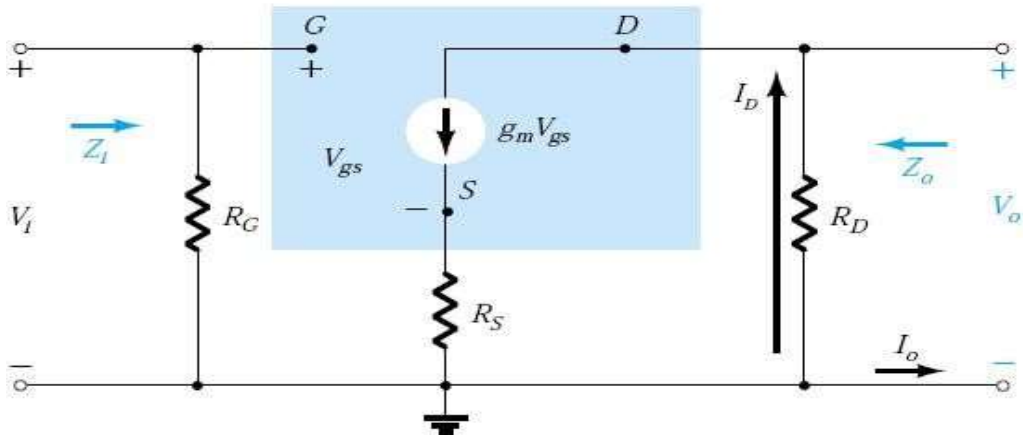
$$Z_i = R_G$$

$$Zo = R_D$$

$$Av = -gmR_D[1+gmRs+(R_D+Rs)/r_d)]$$

5.6   VOLTAGE-DIVIDER CONFIGURATION
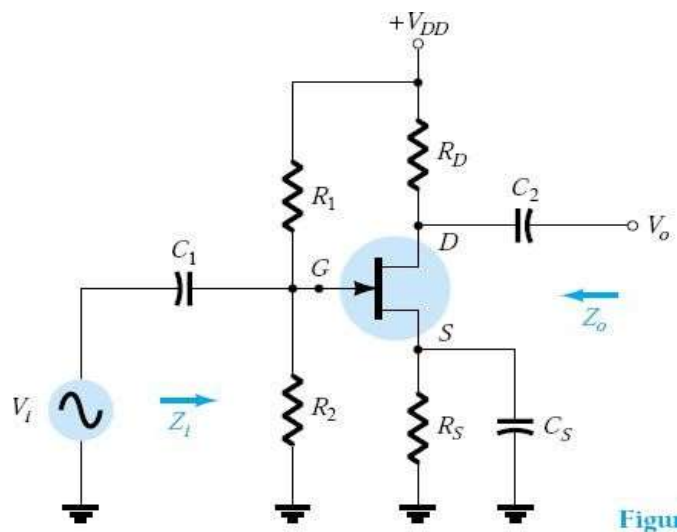
Figu
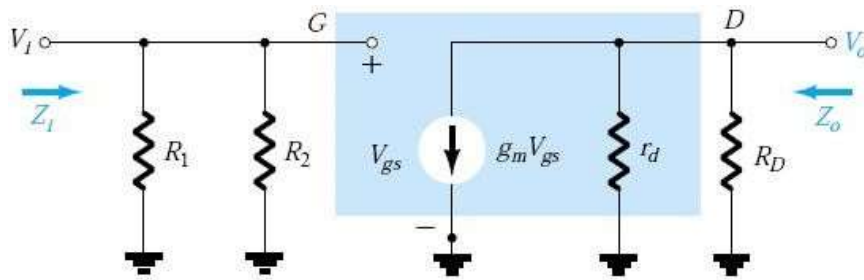
$$Z_i = R1 \| R2$$

$$Z_o = r_d \| R_D$$

$$A_v = -g_m(r_d \| R_D)$$

5.7 SOURCE-FOLLOWER (COMMON-DRAIN) CONFIGURATION
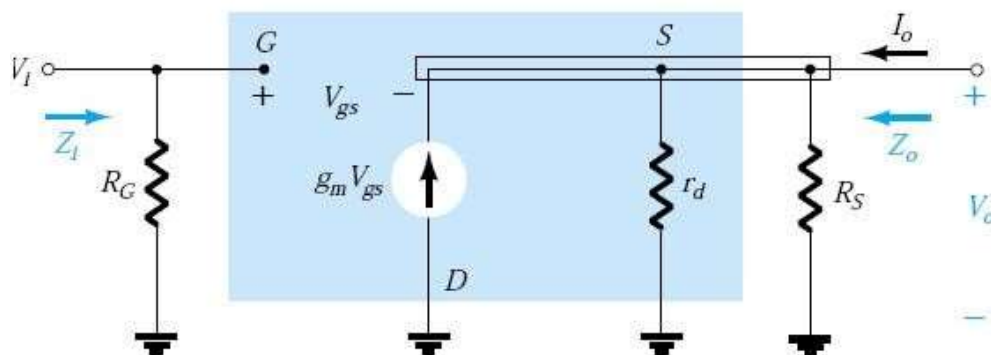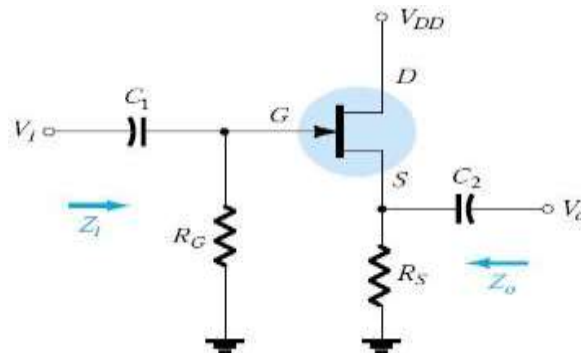
$$Zi = R_G$$

$$Zo = rd\|Rs\|1/gm$$

$$Av = gm(rd\|Rs)/1+gm(rd\|Rs)$$

5.8 COMMON-GATE CONFIGURATION
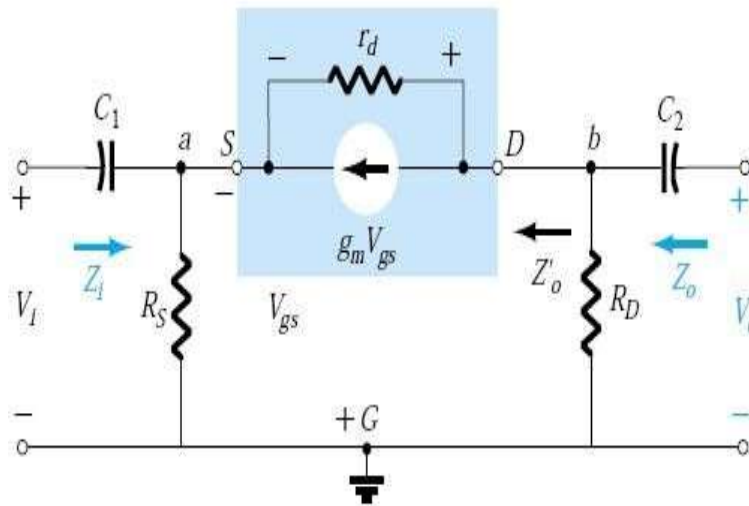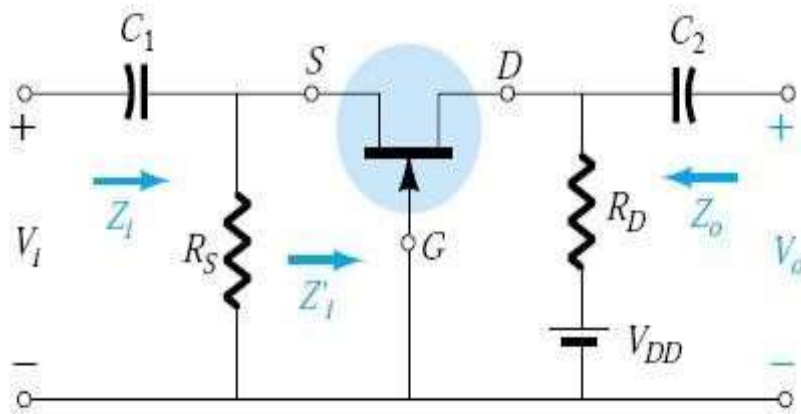
$$Zi = Rs\|[(rd+R_D)/1+gmR_D]$$

$$Zo = rd\|R_D$$

$$Av = [gmR_D+(R_D/rd)]/[1+(R_D/rd)]$$

Chapter 6 HIGH FREQUENCY RESPONSE OF FETS AND BJTS

6.1   LOW-FREQUENCY RESPONSE — BJT AMPLIFIER

The capacitors *Cs*, *CC*, and *CE* will determine the low-frequency response.
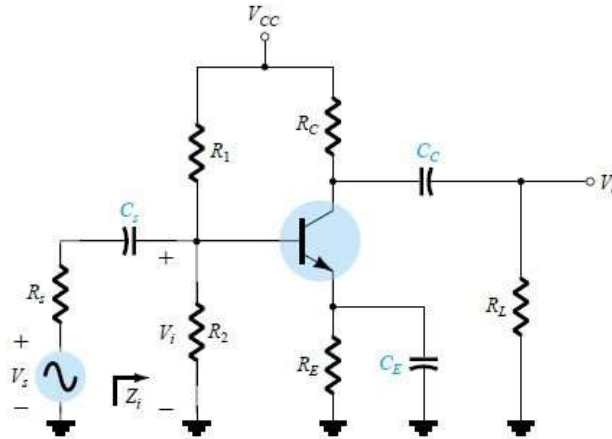
Fig. 6.1 Loaded BJT amplifier with capacitors that affect the low-frequency response

C$_S$:-

Since *Cs* is normally connected between the applied source and the active device, the general form of the *R-C* configuration is established by the network of Fig. 7.2. The total resistance is now *Rs + Ri*.
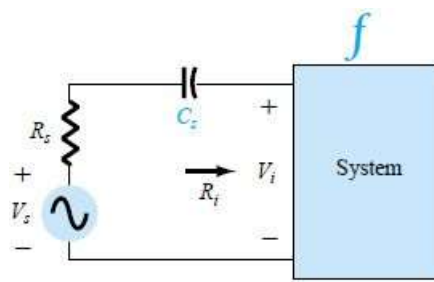
Fig. 6.2 Determining the effect of *Cs* on the low frequency response

$$f_{Ls} = 1/2\pi(Rs+Ri)Cs$$

At mid or high frequencies, the reactance of the capacitor will be sufficiently small to permit a short-circuit approximation for the element. The voltage *Vi* will then be related to *Vs* by

$$Vi|mid = RiVs/(Ri+Rs)$$

At f_{LS}, the voltage Vi will be 70.7% of the value assuming that Cs is the only capacitive element controlling the low-frequency response.
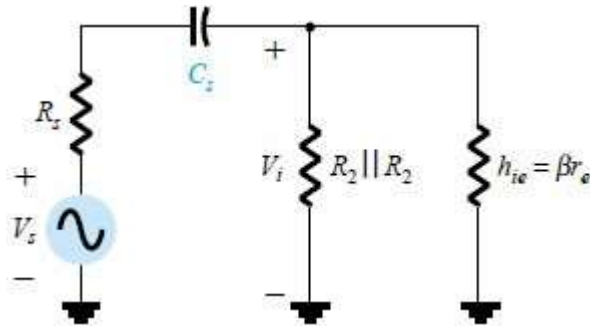
Fig. 6.3 Localized ac equivalent for Cs

Ri = R1||R2||Rs

Vi = RiVs/(Rs+Ri-jXCs)

C_C:-

Since the coupling capacitor is normally connected between the output of the active device and the applied load, the *R-C* configuration that determines the low cut-off frequency due to C_C appears in Fig. 6.4.
The total series resistance is now $Ro + R_L$ and the cut-off frequency due to C_C is determined by

f_{Lc} = 1/2π(Ro+R_L)C_C
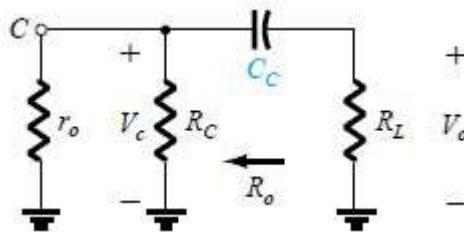
Fig. 6.5 Localized ac equivalent for C_C with Vi =0 V

Ignoring the effects of Cs and C_E, the output voltage Vo will be 70.7% of its mid-band value at f_{LC}. The resulting value for Ro=Rc||ro

C$_E$:-

To determine f_{LE}, the network "seen" by C_E must be determined as shown in Fig. 6.6. Once the level of Re is established, the cut-off frequency due to CE can be determined.
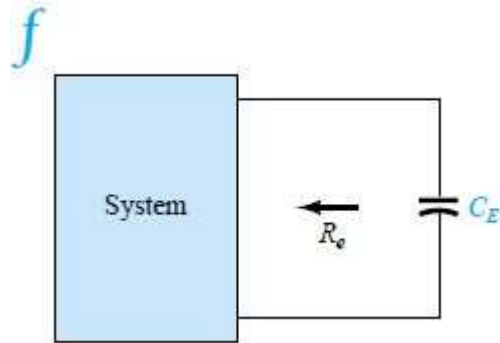
Fig. 6.6 Determining the effect of CE on the low-frequency response

$$f_{LE} = 1/2\pi ReC_E$$
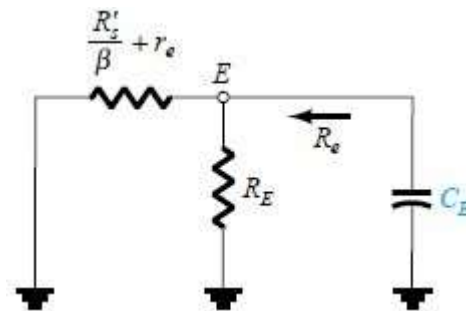
Fig. 6.7 Localized ac equivalent of C_E

$$Re = R_E||(R's/\beta + re)$$

Where, R's = R1||R2||Rs

Before continuing, keep in mind that Cs, C_C, and C_E will affect only the low frequency response. At the mid-band frequency level, the short-circuit equivalents for the capacitors can be inserted. Although each will affect the gain $Av = Vo/Vi$ in a similar frequency range, the highest low-frequency cut-off determined by Cs, C_C, or C_E will have the greatest impact since it will be the last encountered before the mid-band level. If the frequencies are relatively far apart, the highest cut-off frequency will essentially determine the lower cut-off frequency for the entire system. If there are two or more "high" cut-off frequencies, the effect will be to raise the lower cut-off frequency and reduce the resulting bandwidth of the system. In other words, there is an interaction between capacitive elements that can affect the resulting low cut-off frequency.

However, if the cut-off frequencies established by each capacitor are sufficiently separated, the effect of one on the other can be ignored with a high degree of accuracy.

6.2 LOW-FREQUENCY RESPONSE — FET AMPLIFIER

The analysis of the FET amplifier in the low-frequency region will be quite similar to that of the BJT amplifier. There are again three capacitors of primary concern C_G, C_C, and C_S.
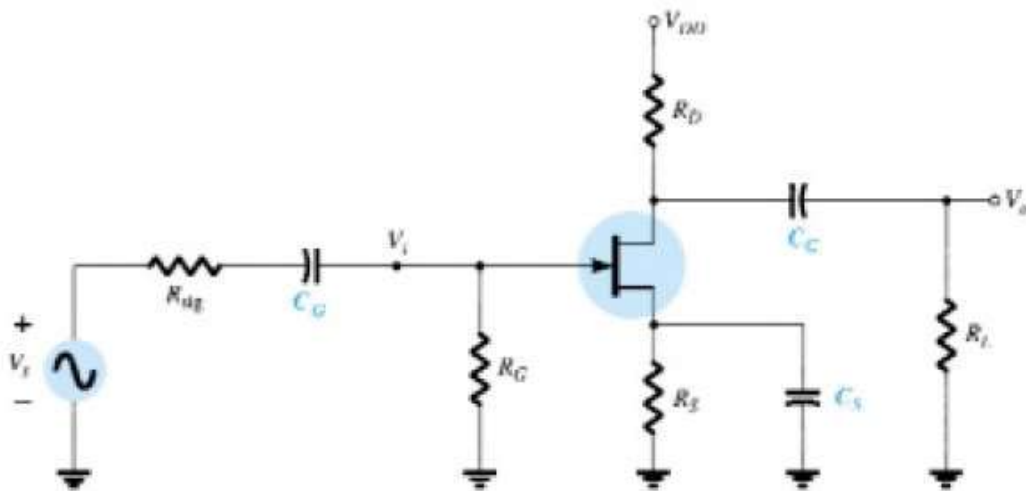
Fig. 6.8 Capacitive elements that affect the low-frequency response of a JFET amplifier

C_G:-

For the coupling capacitor between the source and the active device, the ac equivalent network will appear as shown in Fig. 6.9. The cut-off frequency determined by C_G will be

$$f_{LG} = 1/2\pi(R_{sig}+R_i)C_G$$

where, $R_i = R_G$
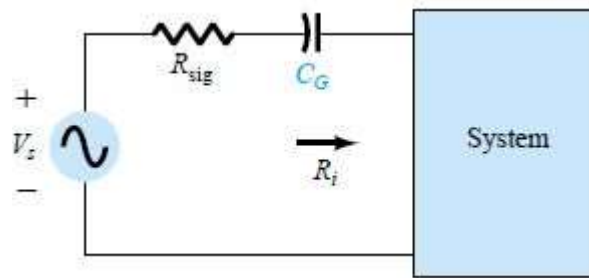
Fig. 6.9 Determining the effect of *CG* on the low-frequency response

C$_C$:-
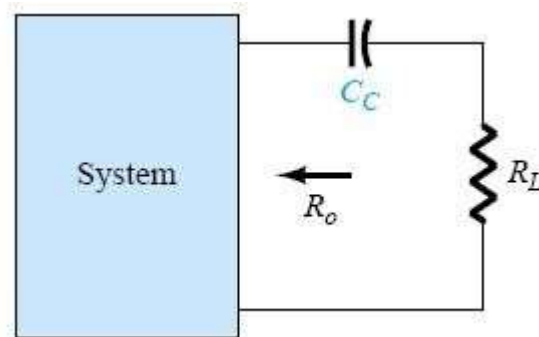
Fig. 6.10 Determining the effect of C_C on the low-frequency response.

$$f_{LC} = 1/2\pi(Ro+R_L)C_C$$

$$Ro = rd||R_D$$

C$_S$:-
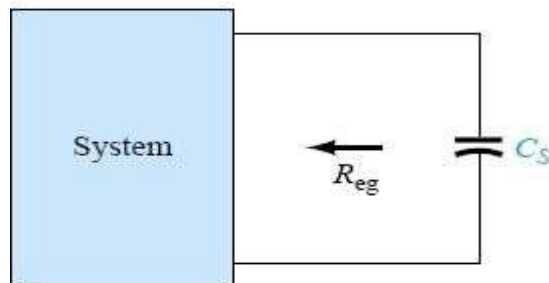
Fig. 6.11 Determining the effect of C$_S$ on the low-frequency response.

$$f_{LS} = 1/2\pi Req C_S$$

$$Req = R_S/1+R_S(1+g_m r_d)/(r_d+R_D\|R_L)$$

6.3   MILLER EFFECT CAPACITANCE

In the high-frequency region, the capacitive elements of importance are the interelectrode (between terminals) capacitances internal to the active device and the wiring capacitance between leads of the network. The large capacitors of the network that controlled the low-frequency response have all been replaced by their short-circuit equivalent due to their very low reactance levels.

For *inverting* amplifiers (phase shift of 180° between input and output resulting in a negative value for *Av*), the input and output capacitance is increased by a capacitance level sensitive to the interelectrode capacitance between the input and output terminals of the device and the gain of the amplifier.
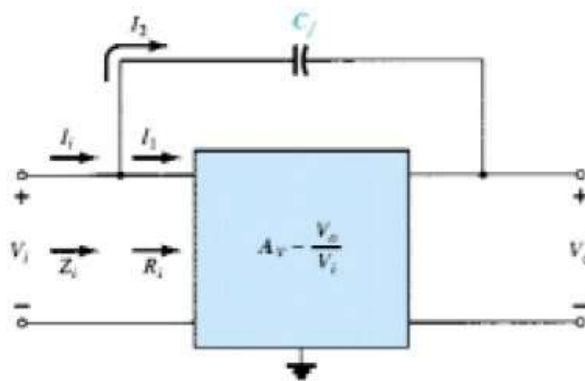
Fig. 6.12 Network employed in the derivation of an equation for the Miller input capacitance

$$\frac{1}{Z_i} = \frac{1}{R_i} + \frac{1}{X_{C_M}}$$
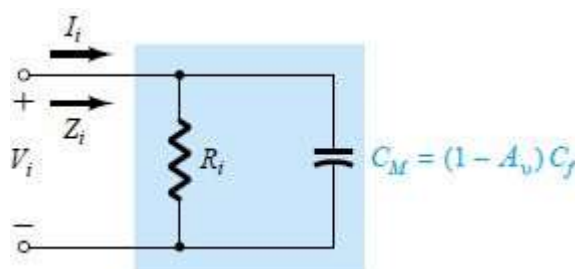
Fig. 6.13 Demonstrating the impact of the Miller effect capacitance.

In general, therefore, the Miller effect input capacitance is defined by

$$C_{Mi} = (1 - Av)C_f$$

This shows us that:

For any inverting amplifier, the input capacitance will be increased by a Miller effect capacitance sensitive to the gain of the amplifier and the interelectrode capacitance connected between the input and output terminals of the active device.
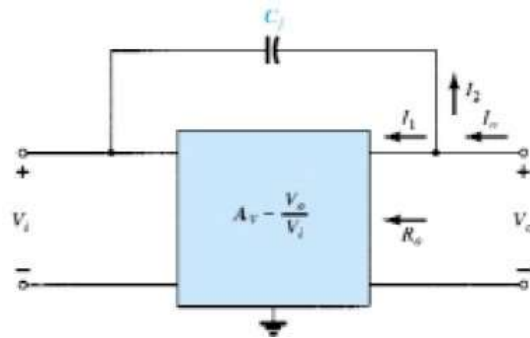
Fig. 6.13 Network employed in the derivation of an equation for the Miller output capacitance

$$C_{Mo} = (1 - 1/Av)C_f$$

Chapter 7 FEEDBACK AND OSCILLATOR CIRCUITS

7.1   FEEDBACK CONCEPTS

Feedback has been mentioned previously. In particular, feedback was used in op-amp circuits as described in Chapters 14 and 15. Depending on the relative polarity of the signal being fed back into a circuit, one may have negative or positive feedback. Negative feedback results in decreased voltage gain, for which a number of circuit features are improved as summarized below. Positive feedback drives a circuit into oscillation as in various types of oscillator circuits. A typical feedback connection is shown in Fig. 7.1. The input signal, Vs, is applied to a mixer network, where it is combined with a feedback signal, V_f. The difference of these signals, V_i, is then the input voltage to the amplifier. A portion of the amplifier output, V_O, is connected to the feedback network (β), which provides a reduced portion of the output as feedback signal to the input mixer network. If the feedback signal is of opposite polarity to the input signal, as shown in Fig. 7.1, negative feedback results. While negative feedback results in reduced overall voltage gain, a number of improvements are obtained, among them being:

1. Higher input impedance.
2. Better stabilized voltage gain.
3. Improved frequency response.
4. Lower output impedance.
5. Reduced noise.
6. More linear operation.
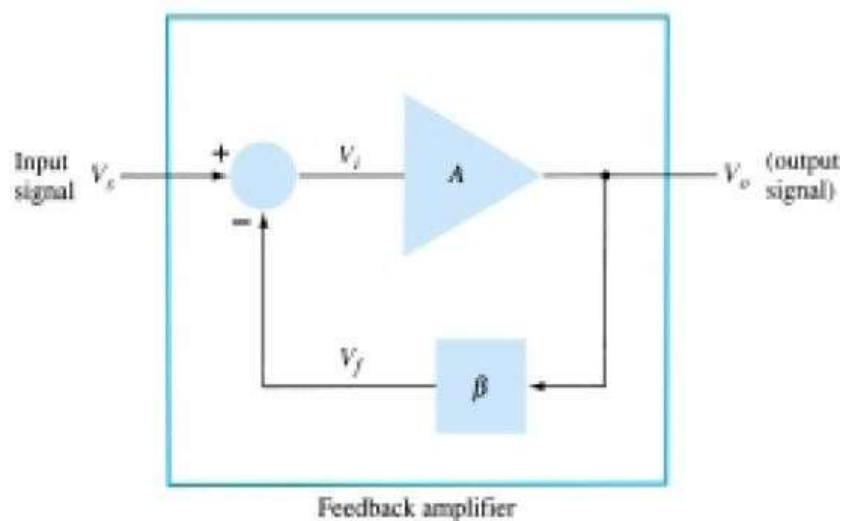
Fig. 7.1 Simple block diagram of feedback amplifier

7.2   FEEDBACK CONNECTION TYPES

There are four basic ways of connecting the feedback signal. Both *voltage* and *current* can be fed back to the input either in *series* or *parallel*. Specifically, there can be:
1. Voltage-series feedback (Fig. 7.2a).
2. Voltage-shunt feedback (Fig. 7.2b).
3. Current-series feedback (Fig. 7.2c).
4. Current-shunt feedback (Fig. 7.2d).

In the list above, *voltage* refers to connecting the output voltage as input to the feedback network; *current* refers to tapping off some output current through the feedback network. *Series* refers to connecting the feedback signal in series with the input signal voltage; *shunt* refers to connecting the feedback signal in shunt (parallel) with an input current source.

Series feedback connections tend to *increase* the input resistance, while shunt feedback connections tend to *decrease* the input resistance. Voltage feedback tends to *decrease* the output impedance, while current feedback tends to *increase* the output impedance. Typically, higher input and lower output impedances are desired for most cascade amplifiers. Both of these are provided using the voltage-series feedback connection.

(a)

(b)
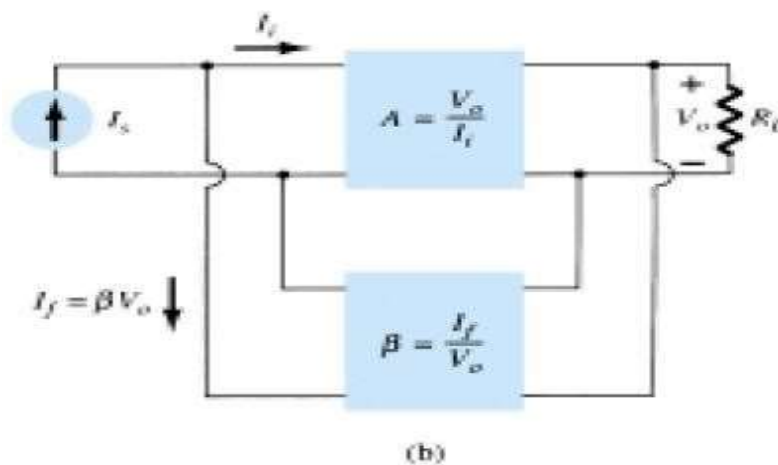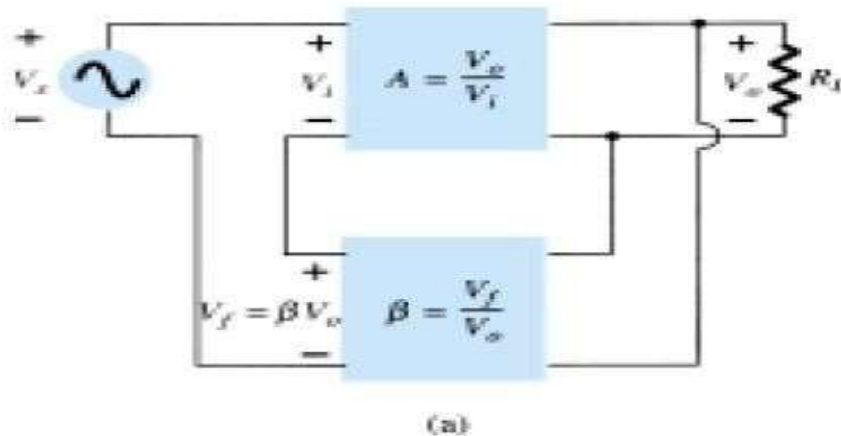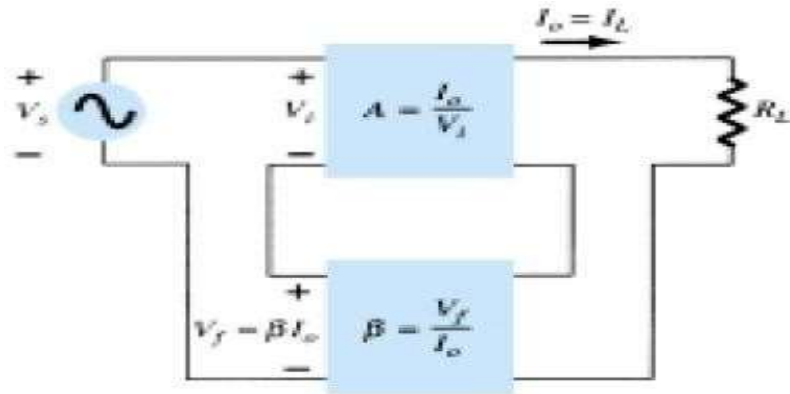
(c)
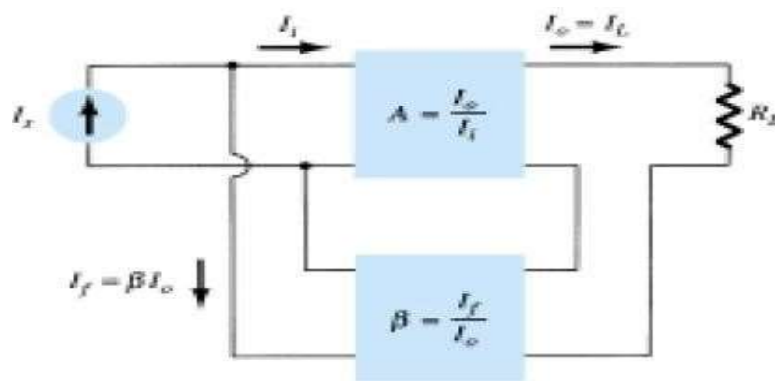
(d)

Fig. 7.2 Feedback amplifier types: (a) voltage-series feedback, $A_f = V_O / V_S$;
(b) voltage-shunt feedback, $A_f = V_O / I_S$;
(c) current-series feedback, $A_f = I_O / V_S$;
(d) current-shunt feedback, $A_f = I_O / I_S$.

Gain with Feedback

In this section we examine the gain of each of the feedback circuit connections of Fig. 7.2. The gain without feedback, A, is that of the amplifier stage. With feedback, β, the overall gain of the circuit is reduced by a factor $(1+\beta A)$, as detailed below. A summary of the gain, feedback factor, and gain with feedback of Fig. 7.2 is provided for reference in Table 7.1.

		Voltage-Series	Voltage-Shunt	Current-Series	Current-Shunt
Gain without feedback	A	$\dfrac{V_o}{V_i}$	$\dfrac{V_o}{I_i}$	$\dfrac{I_o}{V_i}$	$\dfrac{I_o}{I_i}$
Feedback	β	$\dfrac{V_f}{V_o}$	$\dfrac{I_f}{V_o}$	$\dfrac{V_f}{I_o}$	$\dfrac{I_f}{I_o}$
Gain with feedback	A_f	$\dfrac{V_o}{V_s}$	$\dfrac{V_o}{I_s}$	$\dfrac{I_o}{V_s}$	$\dfrac{I_o}{I_s}$

Table 7.1 Summary of Gain, Feedback, and Gain with Feedback from Fig. 7.2

VOLTAGE-SERIES FEEDBACK

Fig 7.2(a) shows the voltage-series feedback connection with a part of the output voltage fed back in series with the input signal, resulting in an overall gain reduction. If there is no feedback ($V_f = 0$), the voltage gain of the amplifier stage is

$A = V_O/V_S = V_O/V_i$ --------------------------- (7.1)

If a feedback signal, V_f, is connected in series with the input, then

$V_i = V_S - V_f$

Since $V_O = AV_i = A(V_S - V_f) = AV_S - AV_f = AV_S - A(\beta V_O)$

Then $(1 + \beta A)V_O = AV_S$

so that the overall voltage gain with feedback is

$A_f = V_O/V_S = A/(1 + \beta A)$ ----------------------- (7.2)

Equation (7.2) shows that the gain with feedback is the amplifier gain reduced by the factor $(1 + \beta A)$. This factor will be seen also to affect input and output impedance among other circuit features.

VOLTAGE-SHUNT FEEDBACK

The gain with feedback for the network of Fig. 7.2(b) is

$A_f = V_O/V_S = AI_i/(I_i + I_f) = AI_i/(I_i + \beta V_O) = AI_i/(I_i + \beta AI_i)$

$A_f = A/(1 + \beta A)$ ------------------------------------- (7.3)

Input Impedance with Feedback

VOLTAGE-SERIES FEEDBACK

A more detailed voltage-series feedback connection is shown in Fig. 7.3. The input impedance can be determined as follows:

$I_i = V_i/Z_i = (V_S - V_f)/Z_i = (V_S - \beta V_O)/Z_i = (V_S - \beta AV_i)/Z_i$

$I_i Z_i = V_S - \beta AV_i$

$V_S = I_i Z_i + \beta AV_i = I_i Z_i + \beta A I_i Z_i$

$Z_{if} = V_S/I_i = Zi + \beta AZi = Zi(1 + \beta A)$----------------------- (7.4)

The input impedance with series feedback is seen to be the value of the input impedance without feedback multiplied by the factor $(1 + \beta A)$ and applies to both voltage- series (Fig. 7.2(a)) and current-series (Fig. 7.2(c)) configurations.
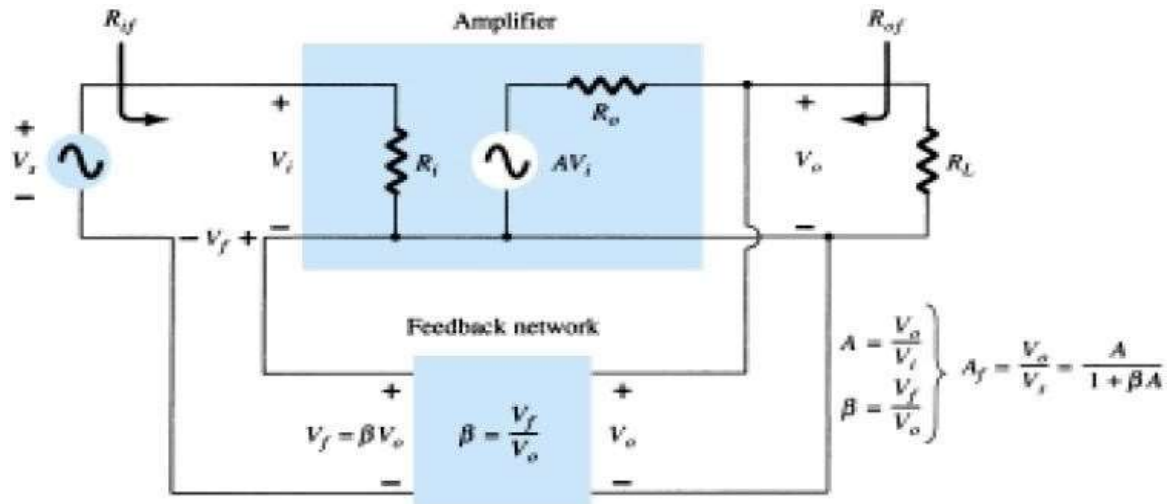
Fig. 7.3 Voltage-Series feedback connection

VOLTAGE-SHUNT FEEDBACK

A more detailed voltage-shunt feedback connection is shown in Fig. 7.4. The input impedance can be determined to be
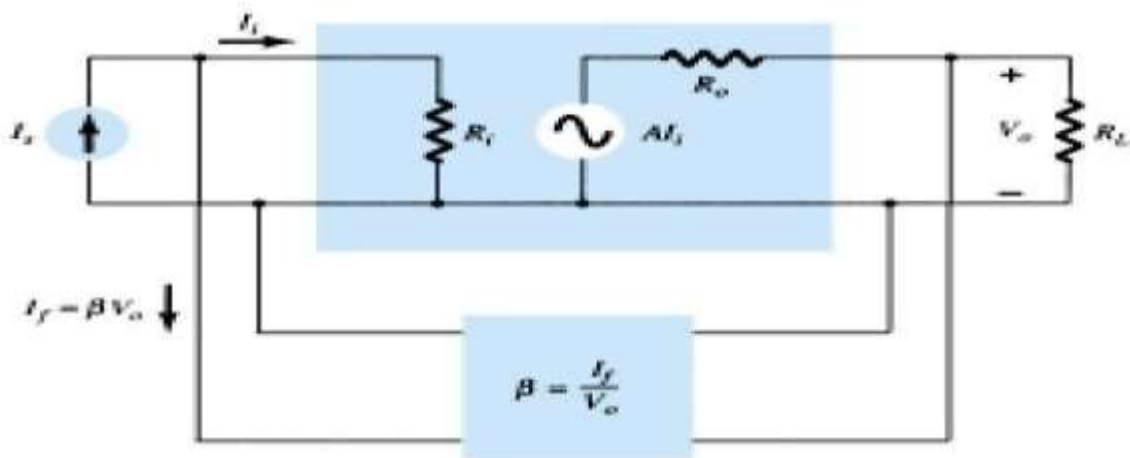
Fig. 7.4 Voltage-Shunt feedback connection

$$Z_{if} = V_i/I_S = V_i/(I_i+I_f) = V_i/(I_i+\beta V_O)$$
$$= (V_f/V_i)/[(I_f/I_i)+(\beta V_O/V_i)]$$
$$Z_{if} = Z_i/(1+\beta A) \text{ ----------------------------------(7.5)}$$

This reduced input impedance applies to the voltage-series connection of Fig. 7.2(a) and the voltage-shunt connection of Fig. 7.2(b)

Output Impedance with Feedback

The output impedance for the connections of Fig. 7.2 are dependent on whether voltage or current feedback is used. For voltage feedback, the output impedance is decreased, while current feedback increases the output impedance.

VOLTAGE-SERIES FEEDBACK

The voltage-series feedback circuit of Fig. 7.3 provides sufficient circuit detail to determine the output impedance with feedback. The output impedance is determined by applying a voltage, V, resulting in a current, I, with V_S shorted out (V_S=0). The voltage V is then

$V = IZ_O + AV_i$
For $V_S = 0$, $V_i = -V_f$
So that, $V = IZ_O - AV_f = IZ_O - A(\beta V)$
Rewriting the equation as, $V + \beta AV = IZ_O$
allows solving for the output resistance with feedback:
$Z_{Of} = V/I = Z_O/(1+\beta A)$ --------------------------- (7.6)
Equation (7.6) shows that with voltage-series feedback the output impedance is reduced from that without feedback by the factor $(1+\beta A)$.

CURRENT-SERIES FEEDBACK

The output impedance with current-series feedback can be determined by applying a signal V to the output with Vs shorted out, resulting in a current *I*, the ratio of V to I being the output impedance. Fig 7.5 shows a more detailed connection with current-series feedback. For the output part of a current-series feedback connection shown in Fig. 7.5, the resulting output impedance is determined as follows. With Vs=0,
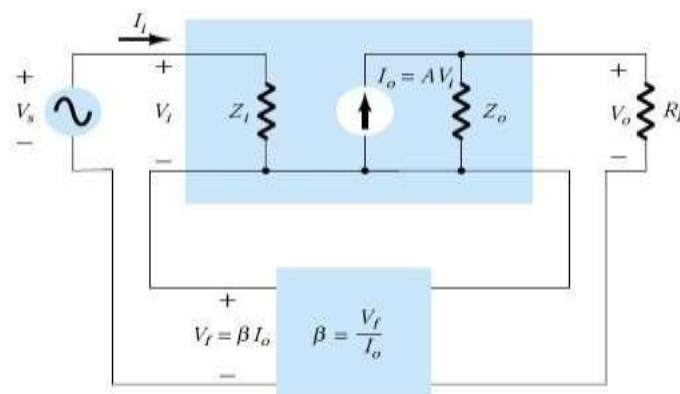
Fig. 7.5 Current-series feedback connection

$V_i = V_f$

$I = V/Z_O - AV_i = V/Z_O - AV_f = V/Z_O - A\beta I$

$Z_O(1+A\beta)I = V$

$Z_{Of} = V/I = Z_O(1+A\beta)$ ------------------- (7.7)

A summary of the effect of feedback on input and output impedance is provided in Table 7.2.

Voltage-Series	Current-Series	Voltage-Shunt	Current-Shunt
Z_{if} $Z_i(1 + \beta A)$ (increased)	$Z_i(1 + \beta A)$ (increased)	$\dfrac{Z_i}{1 + \beta A}$ (decreased)	$\dfrac{Z_i}{1 + \beta A}$ (decreased)
Z_{of} $\dfrac{Z_o}{1 + \beta A}$ (decreased)	$Z_o(1 + \beta A)$ (increased)	$\dfrac{Z_o}{1 + \beta A}$ (decreased)	$Z_o(1 + \beta A)$ (increased)

Table 7.2 Effect of Feedback Connection on Input and Output Impedance

Reduction in Frequency Distortion

For a negative-feedback amplifier having $\beta A \gg 1$, the gain with feedback is $A_f = 1/\beta$. It follows from this that if the feedback network is purely resistive; the gain with feedback is not dependent on frequency even though the basic amplifier gain is frequency dependent. Practically, the frequency distortion arising because of varying amplifier gain with frequency is considerably reduced in a negative-voltage feedback amplifier circuit.

Reduction in Noise and Nonlinear Distortion

Signal feedback tends to hold down the amount of noise signal (such as power-supply hum) and nonlinear distortion. The factor $(1+\beta A)$ reduces both input noise and resulting nonlinear distortion for considerable improvement. However, it should be noted that there is a reduction in overall gain (the price required for the improvement in circuit performance). If additional stages are used to bring the overall gain up to the level without feedback, it should be noted that the extra stage(s) might introduce as much noise back into the system as that reduced by the feedback amplifier. This problem can be somewhat alleviated by readjusting the gain of the feedback-amplifier circuit to obtain higher gain while also providing reduced noise signal.

Effect of Negative Feedback on Gain and Bandwidth

In Eq. (7.2), the overall gain with negative feedback is shown to be

As long as $\beta A >> 1$, the overall gain is approximately $1/\beta$. We should realize that for a practical amplifier (for single low- and high-frequency breakpoints) the open-loop gain drops off at high frequencies due to the active device and circuit capacitances. Gain may also drop off at low frequencies for capacitively coupled amplifier stages. Once the open-loop gain A drops low enough and the factor βA is no longer much larger than 1, the conclusion of Eq. (7.2) that $A_f = 1/\beta$ no longer holds true.

Fig 7.6 shows that the amplifier with negative feedback has more bandwidth (B_f) than the amplifier without feedback (B). The feedback amplifier has a higher upper 3-dB frequency and smaller lower 3-dB frequency.
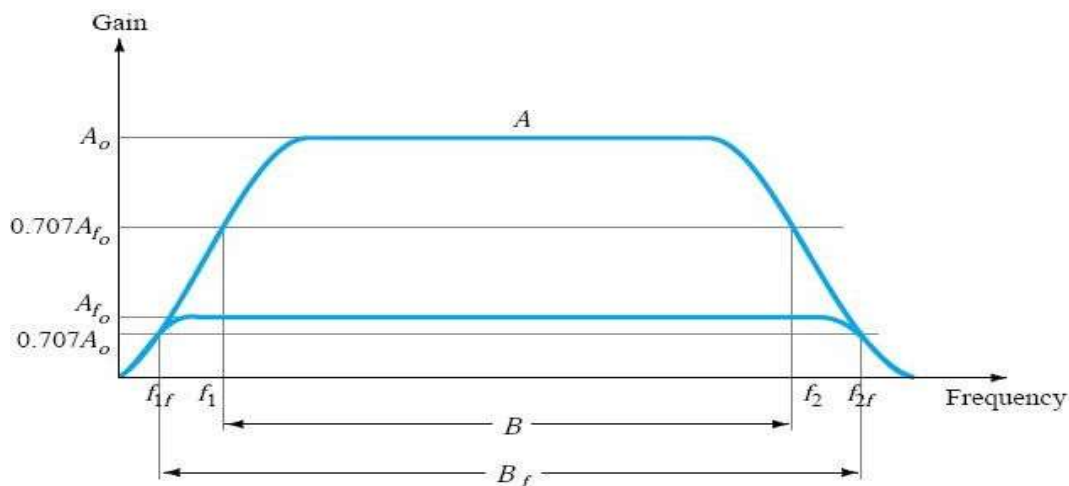
Fig 7.6 Effect of negative feedback on gain and bandwidth

It is interesting to note that the use of feedback, while resulting in a lowering of voltage gain, has provided an increase in *B* and in the upper 3-dB frequency particularly. In fact, the product of gain and frequency remains the same so that the gain–bandwidth product of the basic amplifier is the same value for the feedback amplifier.

However, since the feedback amplifier has lower gain, the net operation was to *trade* gain for bandwidth (we use bandwidth for the upper 3-dB frequency since typically ($f_2 >> f_1$).

Gain Stability with Feedback

In addition to the β factor setting a precise gain value, we are also interested in how stable the feedback amplifier is compared to an amplifier without feedback. Differentiating Eq. (7.2) leads to

$|dA_f/A_f| = [1/ (1+ βA)] / (dA/A)$ ------------------(7.8)
$|dA_f/A_f| = [1/ βA] / [dA/A]$, for $βA>>1$ --------------------- (7.9)

This shows that magnitude of the relative change in gain $|dA_f/A_f|$ is reduced by the factor $|βA|$ compared to that without feedback $(|dA/A|)$.

7.3   PRACTICAL FEEDBACK CIRCUITS

Examples of practical feedback circuits will provide a means of demonstrating the effect feedback has on the various connection types. This section provides only a basic introduction to this topic.

Voltage-Series Feedback

Fig 7.7 shows an FET amplifier stage with voltage-series feedback. A part of the output signal (V_O) is obtained using a feedback network of resistors $R1$ and $R2$. The feedback voltage V_f is connected in series with the source signal V_S, their difference being the input signal V_i. Without feedback the amplifier gain is

$A = V_O/V_i = -g_m R_L$ -----------------------------------(7.10)

where R_L is the parallel combination of resistors:
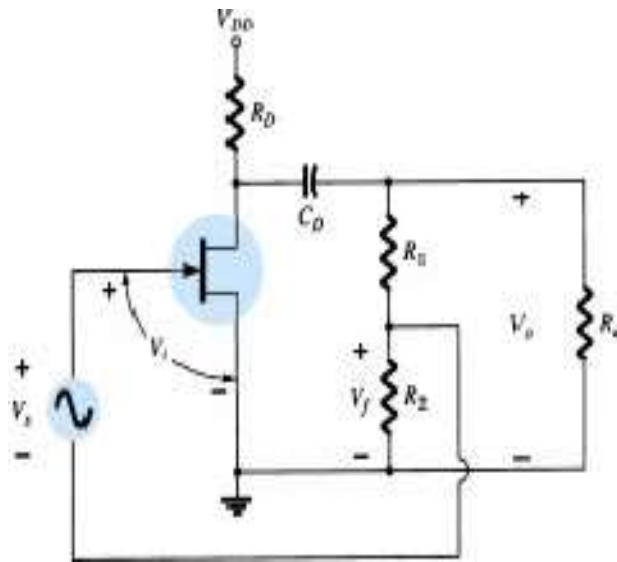
Fig 7.7 FET amplifier stage with voltage-series feedback

$R_L = R_D||R_O||(R_1+R_2)$ --------------------- (7.11)
The feedback network provides a feedback factor of
$β = V_f/V_O = -R_2/(R_1+R_2)$ ------------------------- (7.12)
Using the values of A and _ above in Eq. (7.12), we find the gain with negative feedback to be

$A_f = A/(1+A\beta) = (-g_mRL)/[1+(R_2R_L/(R_1+R_2))g_m]$ ---------------- (7.13)

If we have $\beta A \gg 1$, **$A_f = 1/A\beta = -(R_1+R_2)/R_2$** --------------- (7.14)

Fig 7.8 shows a voltage-series feedback connection using an op-amp. The gain of the op-amp, *A*, without feedback, is reduced by the feedback factor

$\beta = R_2/(R_1+R_2)$ ----------------------- (7.15)
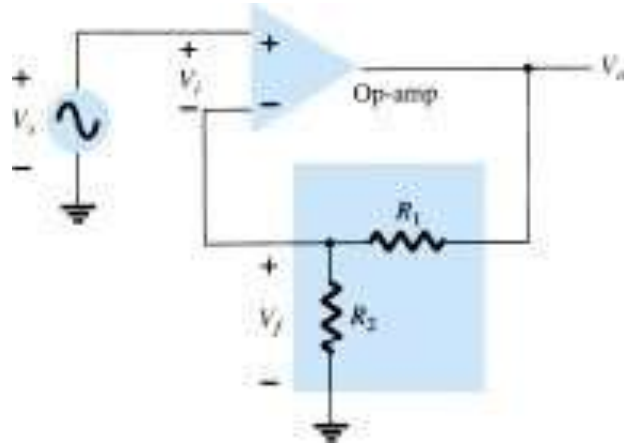
Fig. 7.8 Voltage-series feedback in an op-amp connection

The emitter-follower circuit of Fig. 7.9 provides voltage-series feedback. The signal voltage, V_s, is the input voltage, V_i.
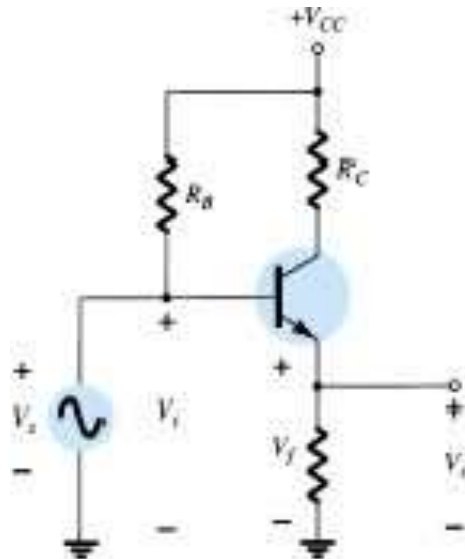
Fig. 7.9 Voltage-series feedback circuit (emitter-follower)

The output voltage, V_o, is also the feed back voltage in series with the input voltage. The amplifier, as shown in Fig. 7.9, provides the operation *with* feedback. The operation of the circuit without feedback provides $V_f = 0$, so that

$A_f = (h_{fe}R_E)/(h_{ie}+h_{fe}R_E)$

For $h_{fe} \gg h_{ie}$,

$A_f = 1$

Current-Series Feedback

Another feedback technique is to sample the output current (Io) and return a proportional voltage in series with the input. While stabilizing the amplifier gain, the current- series feedback connection increases input resistance.
Figure 7.10 shows a single transistor amplifier stage. Since the emitter of this stage has an un-bypassed emitter, it effectively has current-series feedback. The current through resistor RE results in a feedback voltage that opposes the source signal applied so that the output voltage Vo is reduced. To remove the current-series feedback, the emitter resistor must be either removed or bypassed by a capacitor (as is usually done).
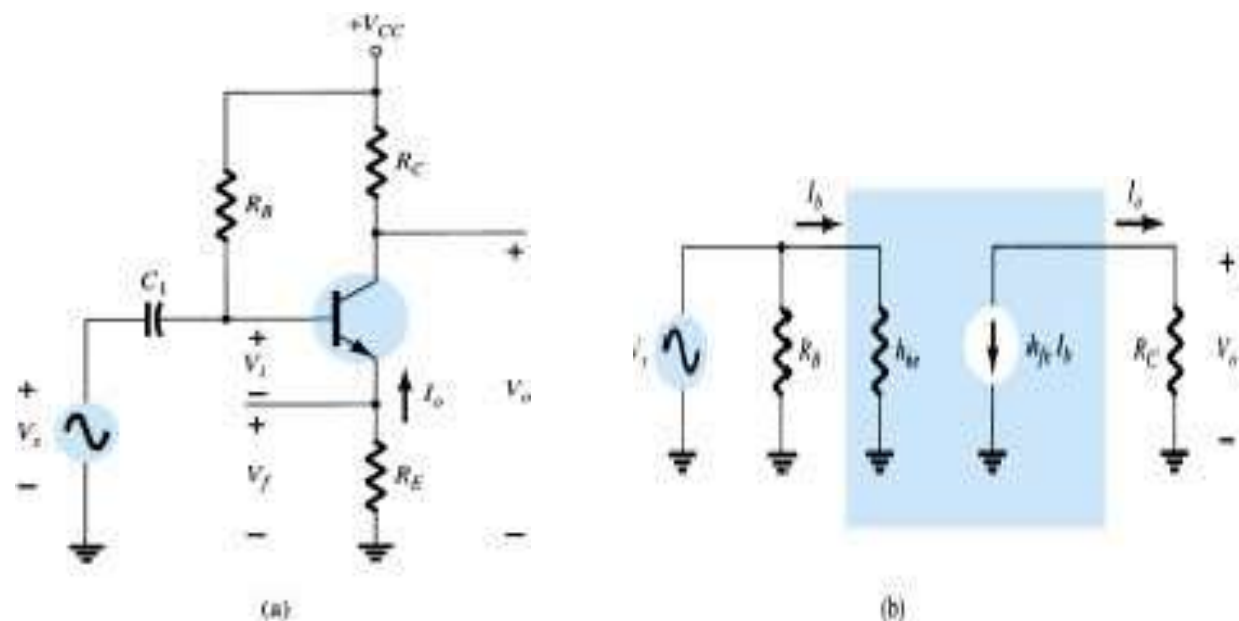
Fig. 7.10 Transistor amplifier with un-bypassed emitter resistor (RE) for current- series feedback: (a) amplifier circuit; (b) ac equivalent circuit without feedback.

WITHOUT FEEDBACK
$A = I_O/V_i = -h_{fe}/(h_{ie}+R_E)$ ---------------- (7.16)
$\beta = V_f/I_O = -R_E$ -------------------------- (7.17)
$Z_i = h_{ie}+R_E$ ------------------------------- (7.18)
$Z_O = R_C$ ---------------------------------- (7.19)

WITH FEEDBACK
$A_f = I_O/V_S = A/(1+A\beta) = -h_{fe}/(h_{ie}+ h_{fe}R_E)$ ----------- (7.20)
$Z_{if} = Z_i(1+A\beta) = h_{ie}+ h_{fe}R_E$ -------------------------------- (7.21)
$Z_{Of} = Z_O(1+A\beta) = R_C(1+ h_{fe}R_E/h_{ie})$ -------------------- (7.22)
$A_{vf} = V_O/V_S = -h_{fe}R_C/(h_{ie}+h_{fe}R_E)$ ----------------------- (7.21)

Voltage-Shunt Feedback

The constant-gain op-amp circuit of Fig. 7.12(a) provides voltage-shunt feedback. Referring to Fig. 7.2(b) and Table 7.1 and the op-amp ideal characteristics $I_i = 0$, $V_i = 0$, and voltage gain of infinity, we have

$A = V_O/V_i = \infty$ -- (7.24)

$\beta = I_f/V_O = -1/R_O$ ------------------------------------- (7.25)

The gain with feedback is then,

$A_f = V_O/I_S = -R_O$ ---------------------------------------(7.26)

This is a transfer resistance gain. The more usual gain is the voltage gain with feedback,

$A_{vf} = (V_O/I_S)(I_S/V_1) = -R_O/R_1$ -------------------------(7.27)
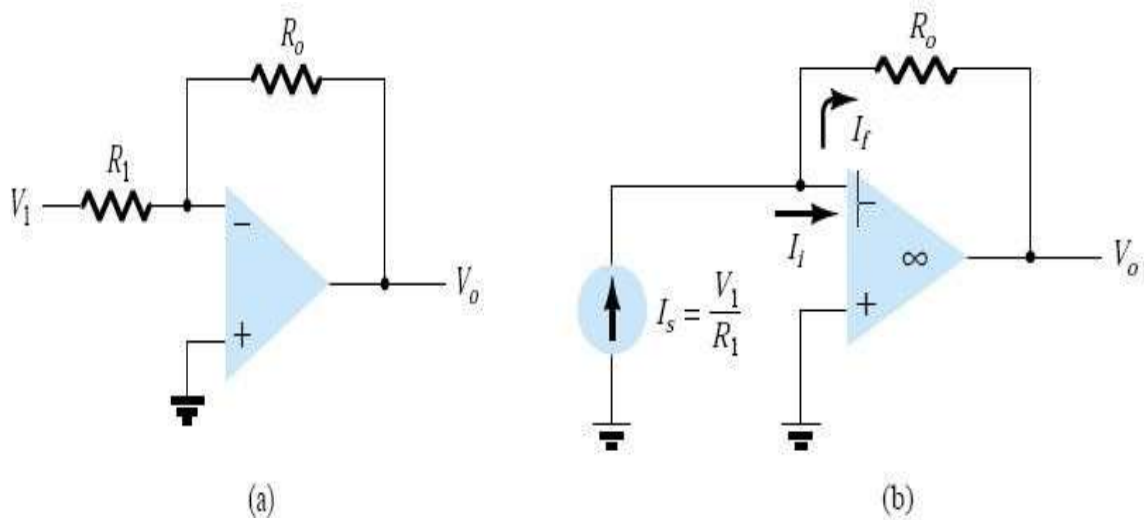
Figure 7.12 Voltage-shunt negative feedback amplifier: (a) constant-gain circuit;(b) equivalent circuit.

The circuit of Fig. 7.13 is a voltage-shunt feedback amplifier using an FET with no feedback, $Vf = 0$

$A = V_O/V_i = -g_m R_D R_S$ ---------------------------- (7.28)

The feedback is,

$\beta = I_f/V_O = -1/R_f$ -------------------------------------(7.29)

With feedback, the gain of the circuit is,

$A_f = V_O/I_S = A/(1+A\beta) = (-g_m R_D R_S R_f)/(R_f + g_m R_D R_S)$ ----------(7.30)

The voltage gain of the circuit with feedback is then,

$A_{vf} = (V_O I_S)/(I_S V_S) = (-g_m R_D R_S R_f)/(R_f + g_m R_D R_S)$-------------- (7.31)
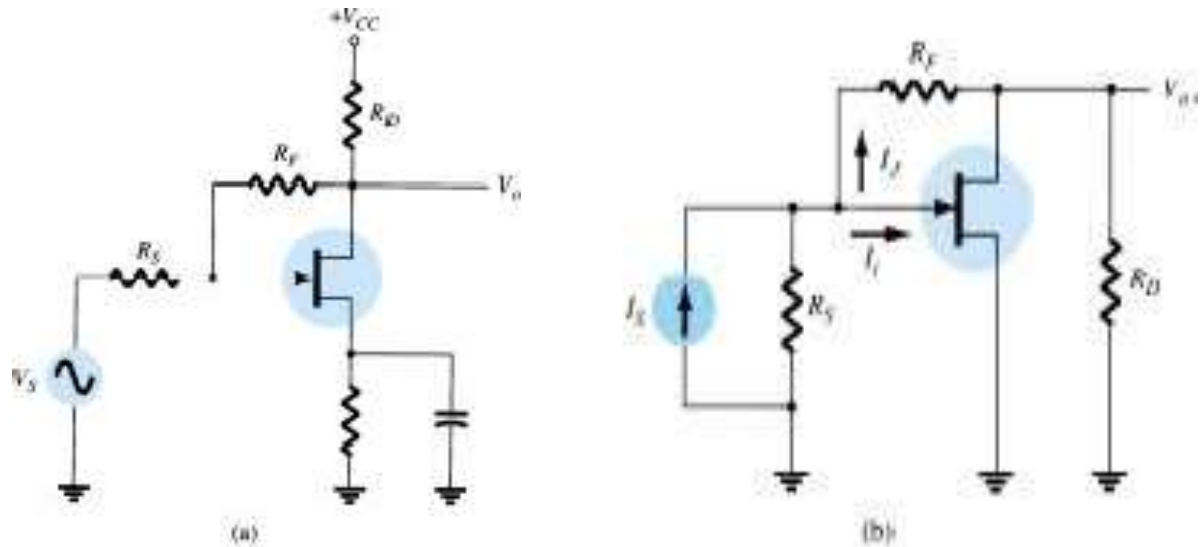
Fig. 7.13 Voltage-shunt feedback amplifier using an FET: (a) circuit; (b) equivalent circuit.

7.4 FEEDBACK AMPLIFIER—PHASE AND FREQUENCY CONSIDERATIONS

So far we have considered the operation of a feedback amplifier in which the feedback signal was *opposite* to the input signal—negative feedback. In any practical circuit this condition occurs only for some mid-frequency range of operation. We know that an amplifier gain will change with frequency, dropping off at high frequencies from the mid-frequency value. In addition, the phase shift of an amplifier will also change with frequency.

If, as the frequency increases, the phase shift changes then some of the feedback signal will *add* to the input signal. It is then possible for the amplifier to break into oscillations due to positive feedback. If the amplifier oscillates at some low or high frequency, it is no longer useful as an amplifier. Proper feedback-amplifier design requires that the circuit be stable at *all* frequencies, not merely those in the range of interest. Otherwise, a transient disturbance could cause a seemingly stable amplifier to suddenly start oscillating.

Nyquist Criterion

In judging the stability of a feedback amplifier, as a function of frequency, the βA product and the phase shift between input and output are the determining factors. One of the most popular techniques used to investigate stability is the Nyquist method. A Nyquist diagram is used to plot gain and phase shift as a function of frequency on a complex plane. The Nyquist plot, in effect, combines the two Bode plots of gain versus frequency and phase shift versus frequency on a single plot. A Nyquist plot is used to quickly show whether an amplifier is stable for all frequencies and how stable the amplifier is relative to some gain or

phase-shift criteria.

As a start, consider the *complex plane* shown in Fig. 7.14. A few points of various gain (βA) values are shown at a few different phase-shift angles. By using the positive real axis as reference (0°), a magnitude of βA = 2 is shown at a phase shift of 0° at point 1. Additionally, a magnitude of βA = 3 at a phase shift of -135° is shown at point 2 and a magnitude/phase of βA = 1 at 180° is shown at point 3. Thus points on this plot can represent *both* gain magnitude of βA and phase shift. If the points representing gain and phase shift for an amplifier circuit are plotted at increasing frequency, then a Nyquist plot is obtained as shown by the plot in Fig. 7.15.

At the origin, the gain is 0 at a frequency of 0 (for *RC*-type coupling). At increasing frequency, points *f*1, *f*2, and *f*3 and the phase shift increased, as did the magnitude of βA. At a representative frequency *f*4, the value of *A* is the vector length from the origin to point *f*4 and the phase shift is the angle φ. At a frequency *f*5, the phase shift is 180°. At higher frequencies, the gain is shown to decrease back to 0.
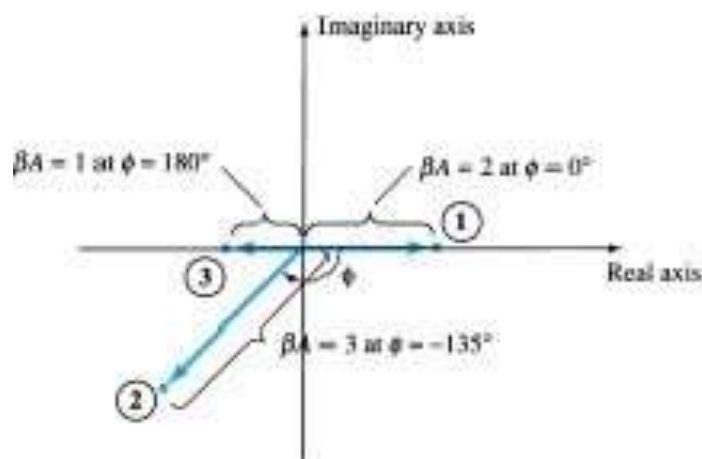
Fig. 7.14 Complex plane showing typical gain-phase points
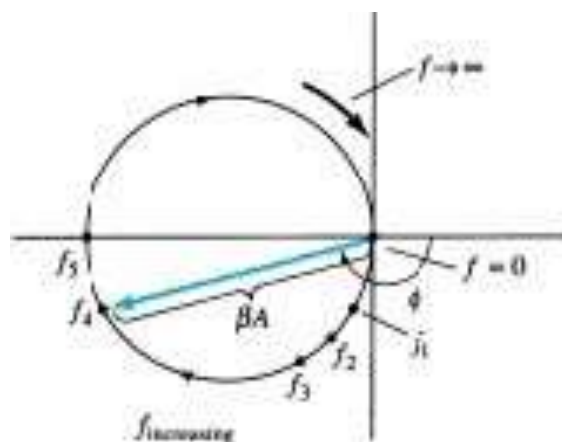
Fig. 7.15 Nyquist Plot

The Nyquist criterion for stability can be stated as follows:
The amplifier is unstable if the Nyquist curve plotted encloses (encircles) the -1 point, and it is stable otherwise.

An example of the Nyquist criterion is demonstrated by the curves in Fig. 7.16. The Nyquist plot in Fig. 7.16(a) is stable since it does not encircle the -1 point, whereas that shown in Fig. 18.16(b) is unstable since the curve does encircle the -1point. Keep in mind that encircling the -1 point means that at a phase shift of 180° the loop gain (βA) is greater than 1; therefore, the feedback signal is in phase with the input and large enough to result in a larger input signal than that applied, with the result that oscillation occurs.

Gain and Phase Margins
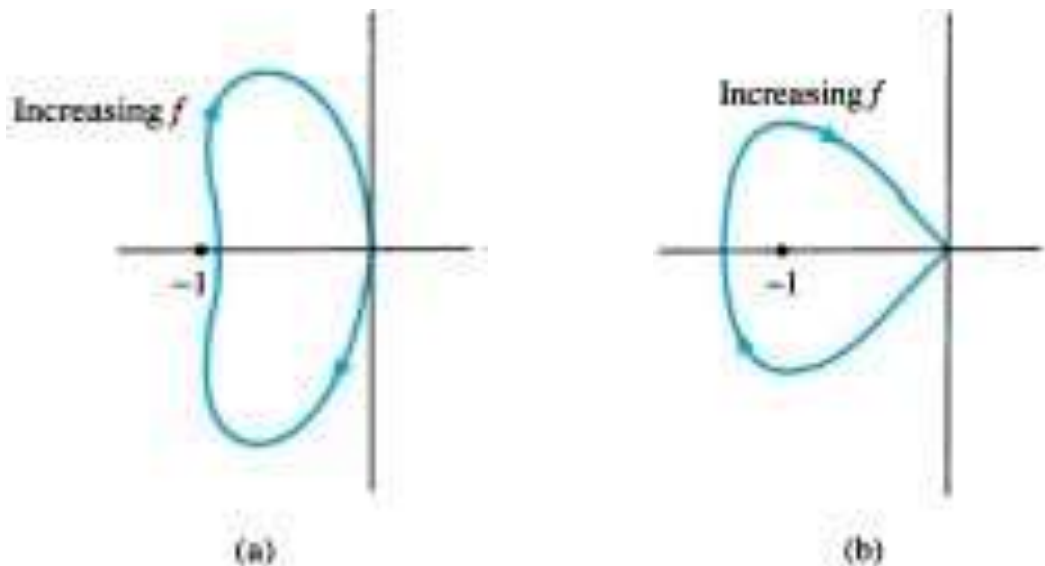
 Fig. 7.16 Nyquist plots showing stability conditions; (a) stable; (b) unstable

From the Nyquist criterion, we know that a feedback amplifier is stable if the loop gain (βA) is less than unity (0 dB) when its phase angle is 180°. We can additionally determine some margins of stability to indicate how close to instability the amplifier is. That is, if the gain (βA) is less than unity but, say, 0.95 in value, this would not be as relatively stable as another amplifier having, say, (βA) = 0.7 (both measured at 180°). Of course, amplifiers with loop gains 0.95 and 0.7 are both stable, but one is closer to instability, if the loop gain increases, than the other.

7.5   OSCILLATOR OPERATION

The use of positive feedback that results in a feedback amplifier having closed-loop gain |Af | greater than 1 and satisfies the phase conditions will result in operation as an oscillator circuit. An oscillator circuit then provides a varying output signal. If the output signal varies sinusoidally, the circuit is referred to as a *sinusoidal oscillator.*

If the output voltage rises quickly to one voltage level and later drops quickly to another voltage level, the circuit is generally referred to as a *pulse* or *square-wave oscillator.*

To understand how a feedback circuit performs as an oscillator, consider the feedback circuit of Fig. 7.18. When the switch at the amplifier input is open, no oscillation occurs. Consider that we have a *fictitious* voltage at the amplifier input (V_i). This results in an output voltage $Vo = AV_i$ after the amplifier stage and in a voltage $V_f = \beta(AV_i)$ after the feedback stage. Thus, we have a feedback voltage $V_f = \beta AV_i$, where βA is referred to as the *loop gain.* If the circuits of the base amplifier and feedback network provide βA of a correct magnitude and phase, V_f can be made equal to V_i.
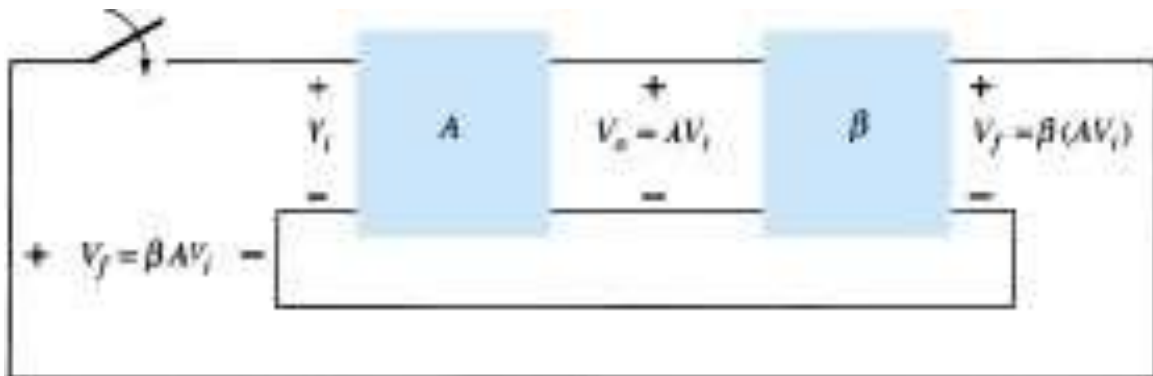
Fig. 7.18 Feedback circuit used as an oscillator

Then, when the switch is closed and fictitious voltage V_i is removed, the circuit will continue operating since the feedback voltage is sufficient to drive the amplifier and feedback circuits resulting in a proper input voltage to sustain the loop operation. The output waveform will still exist after the switch is closed if the condition is met. This is known as the *Barkhausen criterion* for oscillation.

$$\beta A = 1 \text{-------------------------------------- (7.32)}$$

In reality, no input signal is needed to start the oscillator going. Only the condition $\beta A = 1$ must be satisfied for self-sustained oscillations to result. In practice, βA is made greater than 1 and the system is started oscillating by amplifying noise voltage, which is always present. Saturation factors in the practical circuit provide an "average" value of βA of 1. The resulting waveforms

are never exactly sinusoidal. However, the closer the value βA is to exactly 1, the more nearly sinusoidal is the waveform.

7.6   PHASE-SHIFT OSCILLATOR

An example of an oscillator circuit that follows the basic development of a feedback circuit is the *phase-shift oscillator.* An idealized version of this circuit is shown in Fig. 7.20. Recall that the requirements for oscillation are that the loop gain, βA, is greater than unity *and* that the phase shift around the feedback network is 180° (providing positive feedback). In the present idealization, we are considering the feedback network to be driven by a perfect source (zero source impedance) and the output of the feedback network to be connected into a perfect load (infinite load impedance).
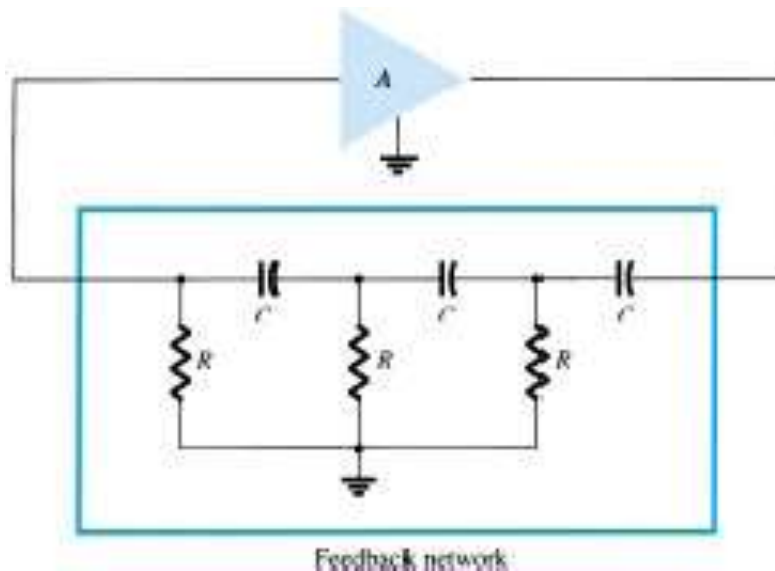
Fig. 7.20 Idealized Phase-Shift Oscillator

Concentrating our attention on the phase-shift network, we are interested in the attenuation of the network at the frequency at which the phase shift is exactly 180°. Using classical network analysis, we find that

$$f = 1/2\pi R_C(6)^{0.5} \text{-----------------------} \quad (7.33)$$
$$\beta = 1/29 \text{----------------------------} \quad (7.34)$$

and the phase shift is 180°.
For the loop gain βA to be greater than unity, the gain of the amplifier stage must be greater than 1/β or 29:
A>29 -----------------------(7.35)
When considering the operation of the feedback network, one might naively select the values of *R* and *C* to provide (at a specific frequency) 60°-phase shift per section for three sections, resulting in a 180° phase shift, as desired. This, however, is not the case, since each section of the *RC* in the feedback network

loads down the previous one. The net result that the *total* phase shift be 180° is all that is important.

The frequency given by Eq. (7.33) is that at which the *total* phase shift is 180°. If one measured the phase shift per *RC* section, each section would not provide the same phase shift (although the overall phase shift is 180°). If it were desired to obtain exactly a 60° phase shift for each of three stages, then emitter-follower stages would be needed for each *RC* section to prevent each from being loaded from the following circuit.

FET Phase-Shift Oscillator

A practical version of a phase-shift oscillator circuit is shown in Fig. 7.21(a). The circuit is drawn to show clearly the amplifier and feedback network. The amplifier stage is self-biased with a capacitor bypassed source resistor R_S and a drain bias resistor R_D. The FET device parameters of interest are g_m and r_d. From FET amplifier theory, the amplifier gain magnitude is calculated from

$|A| = g_m R_L$ -----------------------(7.36)

where R_L in this case is the parallel resistance of R_D and r_d

$R_L = R_D r_d / R_D + r_d$ ---------------- (7.37)

We shall assume as a very good approximation that the input impedance of the FET amplifier stage is infinite. This assumption is valid as long as the oscillator operating frequency is low enough so that FET capacitive impedances can be neglected. The output impedance of the amplifier stage given by R_L should also be small compared to the impedance seen looking into the feedback network so that no attenuation due to loading occurs. In practice, these considerations are not always negligible, and the amplifier stage gain is then selected somewhat larger than the needed factor of 29 to assure oscillator action.
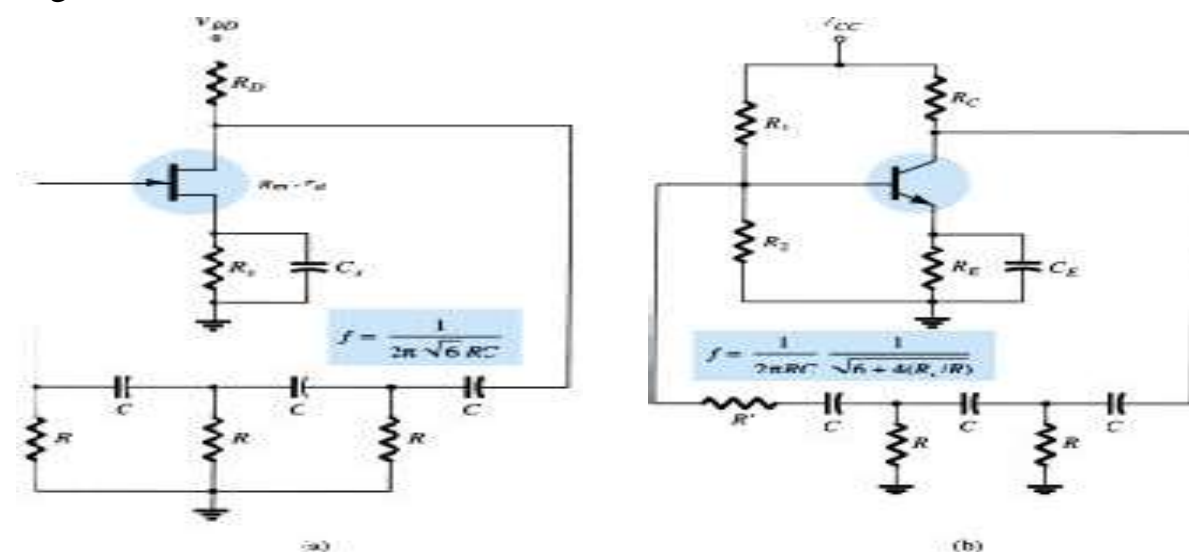
Fig. 7.21 Practical phase-shift oscillator circuits: (a) FET version; (b) BJT version.

Transistor Phase-Shift Oscillator

If a transistor is used as the active element of the amplifier stage, the output of the feedback network is loaded appreciably by the relatively low input resistance (h_{ie}) of the transistor. Of course, an emitter-follower input stage followed by a common-emitter amplifier stage could be used. If a single transistor stage is desired, however, the use of voltage-shunt feedback (as shown in Fig. 7.21(b) is more suitable. In this connection, the feedback signal is coupled through the feedback resistor R' in *series* with the amplifier stage input resistance (R_i). Analysis of the ac circuit provides the following equation for the resulting oscillator frequency:

$$f = (1/2\pi RC)[1/(6+4(R_C/R))^{0.5}] \text{------------------}(7.38)$$

For the loop gain to be greater than unity, the requirement on the current gain of the transistor is found to be

$$h_{fe} > 23+29(R/R_C)+4(R_C/R) \text{-------------------} (7.39)$$

IC Phase-Shift Oscillator

As IC circuits have become more popular, they have been adapted to operate in oscillator circuits. One need buy only an op-amp to obtain an amplifier circuit of stabilized gain setting and incorporate some means of signal feedback to produce an oscillator circuit. For example, a phase-shift oscillator is shown in Fig. 7.22. The output of the op-amp is fed to a three-stage RC network, which provides the needed 180° of phase shift (at an attenuation factor of 1/29). If the op-amp provides gain (set by resistors R_i and R_f) of greater than 29, a loop gain greater than unity results and the circuit acts as an oscillator [oscillator frequency is given by Eq. (7.33).
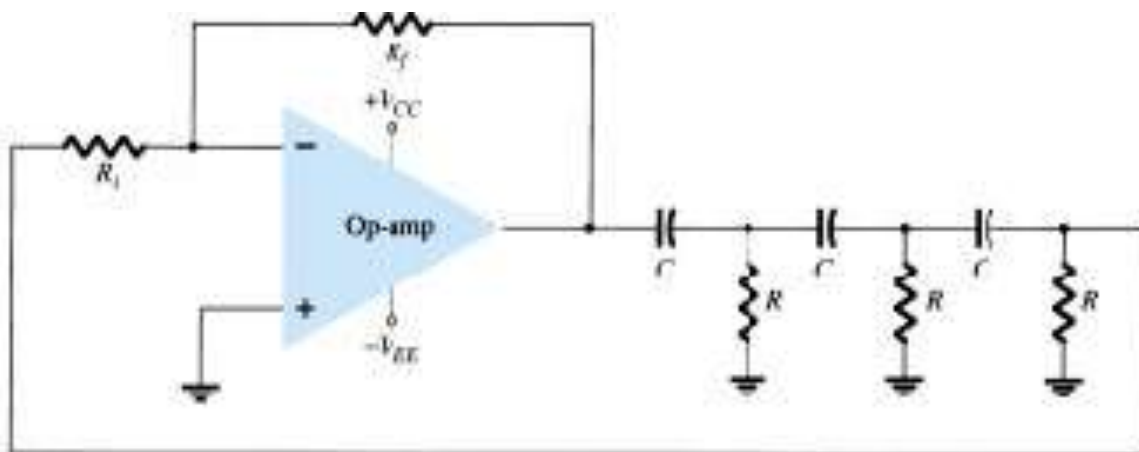
Fig. 7.22 Phase-shift oscillator using op-amp

<u>7.7</u>   <u>WIEN BRIDGE OSCILLATOR</u>

A practical oscillator circuit uses an op-amp and *RC* bridge circuit, with the oscillator frequency set by the *R* and *C* components. Figure 7.23 shows a basic version of a Wien bridge oscillator circuit. Note the basic bridge connection. Resistors R_1 and R_2 and capacitors C_1 and C_2 form the frequency-adjustment elements, while resistors R_3 and R_4 form part of the feedback path. The op-amp output is connected as the bridge input at points *a* and *c*. The bridge circuit output at points *b* and *d* is the input to the op-amp.
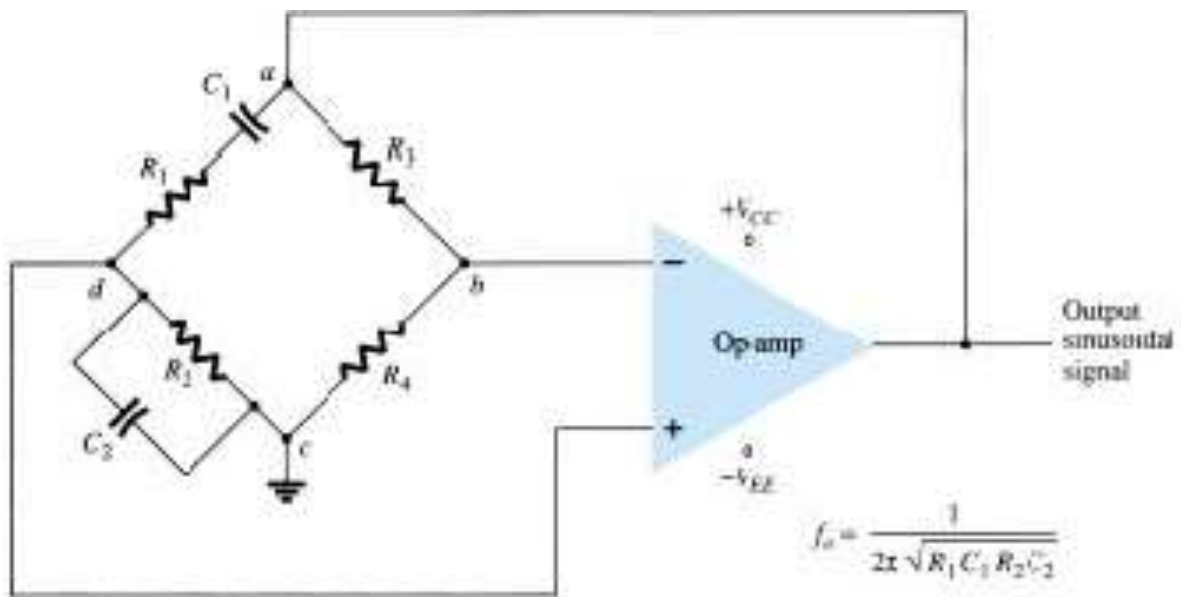
Fig. 7.23 Wien bridge oscillator circuit using op-amp amplifier

Neglecting loading effects of the op-amp input and output impedances, the analysis of the bridge circuit results in
$R_3/R_4 = R_1/R_2 + C_2/C_1$------------------------------- (7.40)
                And $\mathbf{f_0 = 1/2\pi(R_1R_2C_1C_2)^{0.5}}$ ------------------------ (7.41)
If, in particular, the values are $R_1=R_2=R$ and $C_1=C_2=C$, the resulting oscillator frequency is
$f_0 = 1/2\pi RC$--------------------------------- (7.42)
and $R_3/R_4 = 2$----------------------------- (7.43)
Thus a ratio of R_3 to R_4 greater than 2 will provide sufficient loop gain for the circuit to oscillate at the frequency calculated using Eq. (7.42).

7.8   CRYSTAL OSCILLATOR

A crystal oscillator is basically a tuned-circuit oscillator using a piezoelectric crystal as a resonant tank circuit. The crystal (usually quartz) has a greater stability in holding constant at whatever frequency the crystal is originally cut to operate. Crystal oscillators are used whenever great stability is required, such as in communication transmitters and receivers.

Characteristics of a Quartz Crystal

A quartz crystal (one of a number of crystal types) exhibits the property that when mechanical stress is applied across the faces of the crystal, a difference of potential develops across opposite faces of the crystal. This property of a crystal is called the *piezoelectric effect.* Similarly, a voltage applied across one set of faces of the crystal causes mechanical distortion in the crystal shape.
When alternating voltage is applied to a crystal, mechanical vibrations are set up—these vibrations having a natural resonant frequency dependent on the crystal.
Although the crystal has electromechanical resonance, we can represent the crystal action by an equivalent electrical resonant circuit as shown in Fig. 18.31. The inductor L and capacitor C represent electrical equivalents of crystal mass and compliance, while resistance R is an electrical equivalent of the crystal structure's internal friction. The shunt capacitance C_M represents the capacitance due to mechanical mounting of the crystal. Because the crystal losses, represented by R, are small, the equivalent crystal Q (quality factor) is high—typically 20,000. Values of Q up to almost 106 can be achieved by using crystals. The crystal as represented by the equivalent electrical circuit of Fig. 7.31 can have two resonant frequencies. One resonant condition occurs when the reactances of the series RLC leg are equal (and opposite). For this condition, the *series-resonant* impedance is very low (equal to R). The other resonant condition occurs at a higher frequency when the reactance of the series-resonant leg equals the reactance of capacitor C_M. This is a parallel resonance or antiresonance condition of the crystal. At this frequency, the crystal offers a very high impedance to the external circuit.
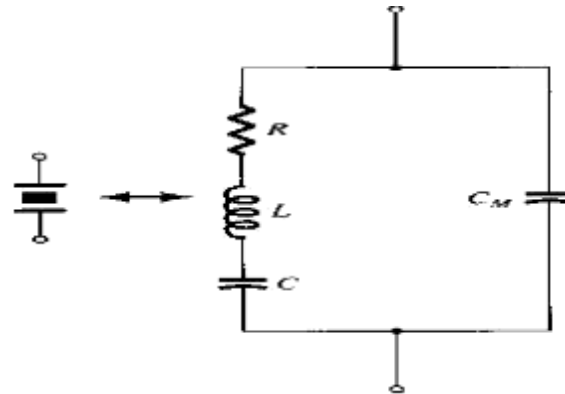
Fig. 7.31 Electrical equivalent circuit of a crystal

The impedance versus frequency of the crystal is shown in Fig. 7.32. In order to use the crystal properly, it must be connected in a circuit so that its low impedance in the series- resonant operating mode or high impedance in the anti-resonant operating mode is selected.
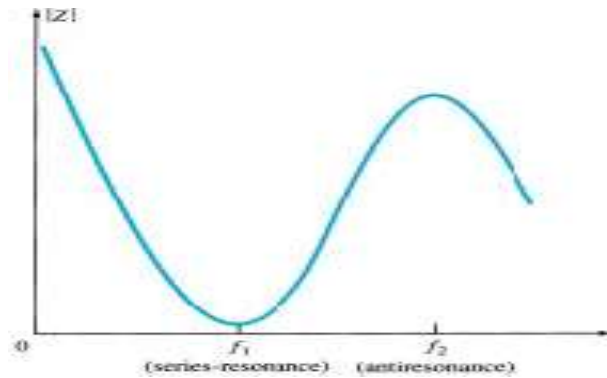
Fig 7.32 Crystal impedance versus frequency

Crystal Oscillator

An op-amp can be used in a crystal oscillator as shown in Fig. 7.36. The crystal is connected in the series-resonant path and operates at the crystal series-resonant frequency. The present circuit has a high gain so that an output square-wave signal results as shown in the figure. A pair of Zener diodes is shown at the output to provide output amplitude at exactly the Zener voltage (V_Z).
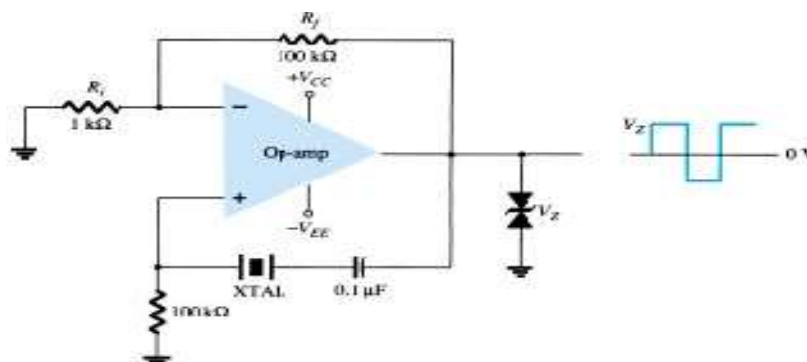
Fig. 7.36 Crystal Oscillator using opamp

Chapter 8   OPERATIONAL AMPLIFIER

8.1   IDEAL OP-AMP

Properties of Ideal Op-amp:

1. Infinite Open Loop Voltage Gain

   $A_{VL} = Vo / V2 – V1 = \infty$

2. Infinte Input Impedance

   $Zi = \infty$

3. Zero Output Impedance

   $Zo = 0$

4. Infinite Bandwidth

   $BW = \infty$

5. Zero Offset

6. Infinite CMRR

   $CMRR = A_d/A_c = \infty$

7. Infinity Slew-Rate

   $SR = dVo/dt = \infty$

8.2   OP-AMP PARAMETERS

1. Common Mode Rejection Ratio (CMRR)

   It is the ratio of differential gain to the common mode gain.
   $CMRR = Ad/Ac$
   $CMRRdb = 20log [Ad/Ac]$

We can express the output voltage in terms of the value of CMRR as follows:

Vo = AdVd(1+1/CMRR*Vc/Vd)

2. Slew-Rate (SR)

It is the maximum rate at which amplifier output can change in volts per microsecond (V/ μs). It is the maximum rate of change of o/p voltage for all possible i/p signals.

SR = dVo/dt V/μs = $2\pi fmax(Vo)_{max}$

8.3 NON-INVERTING CONFIGURATIONS

Inverting Amplifier –

The most widely used constant-gain amplifier circuit is the inverting amplifier.

Here, V1 (or input signal) is connected to the inverting terminal or the – ve terminal. The output is obtained by multiplying the input by a fixed or constant gain, set by the input resistor (*R*1) and feedback resistor (*Rf*).This output also being inverted from the input. It is more widely used because it has better frequency stability.

It is a Transresistance amplifier or (I to V converter).
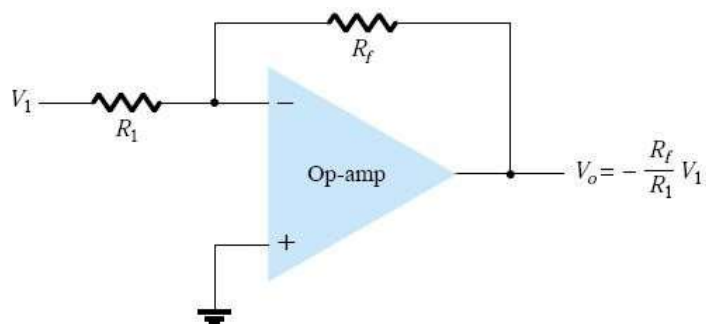
$$V_o = -\frac{R_f}{R_1} V_1$$

Vo = - (Rf/R1) V1

Non-Inverting Amplifier –

Here, the V1 (or input signal) is connected to the non-inverting terminal or the +ve terminal. It is a Voltage amplifier or (V to V converter).
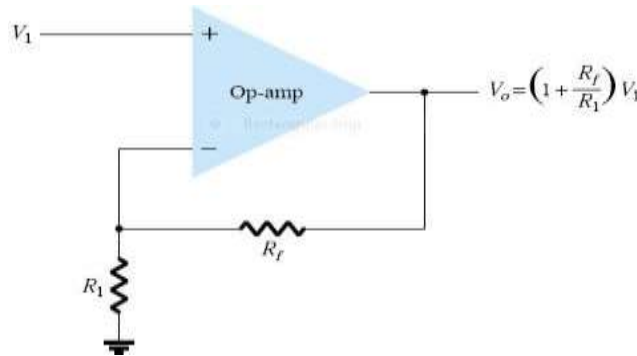
$$V_o = (1 + R_f/R_1) \, V_1$$

Unity Follower Amplifier –

It is otherwise known as Buffer circuit or Voltage follower circuit. The unity-follower circuit, as shown in the below figure, provides a gain of unity (1) with no polarity or phase reversal. From the circuit it is clear that the output is of the same polarity and magnitude as the input. The circuit operates like an emitter- or source-follower circuit except that the gain is exactly unity.
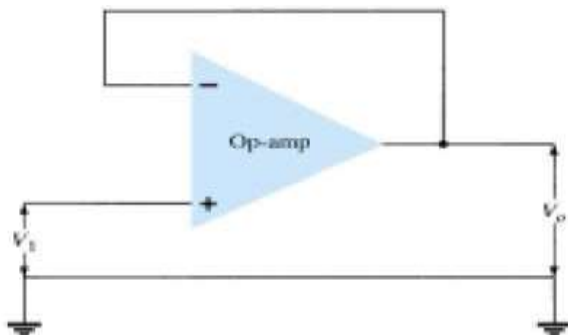
$$V_o = V_1$$

Summing Amplifier –

It is the most used of the op-amp circuits. The below circuit shows a three-input summing amplifier circuit, which provides a means of algebraically summing (adding) three voltages, each multiplied by a constant-gain factor. Here, each input adds a voltage to the output multiplied by its separate constant- gain multiplier. If more inputs are used, they each add an additional component to the output.
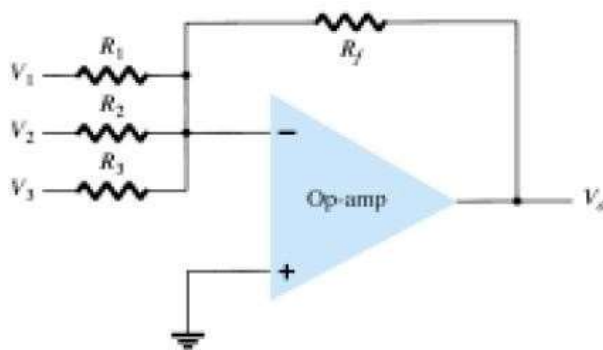
$$Vo = - (Rf/R1 \; x \; V1 + Rf/R2 \; x \; V2 + Rf/R3 \; x \; V3)$$

Integrator –

So far, the input and feedback components have been resistors. But here, the feedback component used is a capacitor, as shown in figure below. The resulting connection is called an integrator.
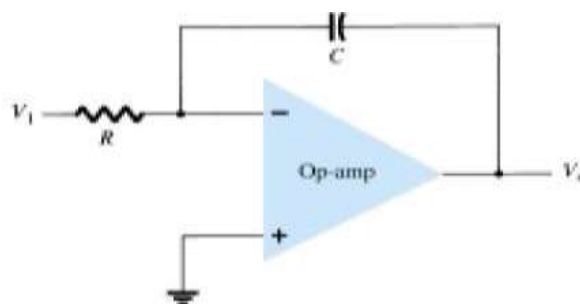
$$Vo(t) = - 1/RC \int V1(t)dt$$

Differentiator –

A differentiator circuit is shown in figure. While not as useful as the circuit forms covered above, the differentiator does provide a useful operation.
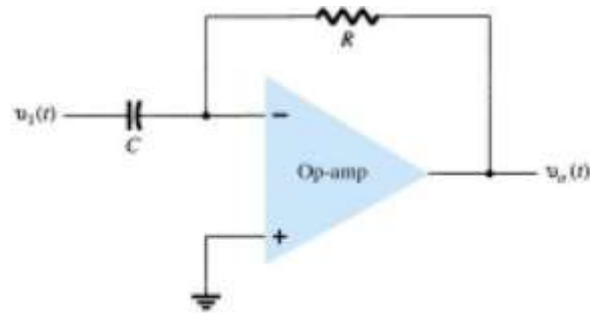
$$Vo(t) = -RC \, dV1(t)/dt$$

Chapter 9   POWER AMPLIFIER

9.1 INTRODUCTION—DEFINITIONS AND AMPLIFIER TYPES

Large-signal or power amplifiers, on the other hand, primarily provide sufficient power to an output load to drive a speaker or other power device, typically a few watts to tens of watts. we concentrate on those amplifier circuits used to handle large-voltage signals at moderate to high current levels. The main features of a large-signal amplifier are the circuit's power efficiency, the maximum amount of power that the circuit is capable of handling, and the impedance matching to the output device. One method used to categorize amplifiers is by class. Basically, amplifier classes represent the amount the output signal varies over one cycle of operation for a full cycle of input signal.

CLASS-A AMPLIFIER: The output signal varies for a full 360° of the cycle. Fig. 9.1(a) shows that this requires the Q-point to be biased at a level so that at least half the signal swing of the output may vary up and down without going to a high-enough voltage to be limited by the supply voltage level or too low to approach the lower supply level, or 0 V in this description.
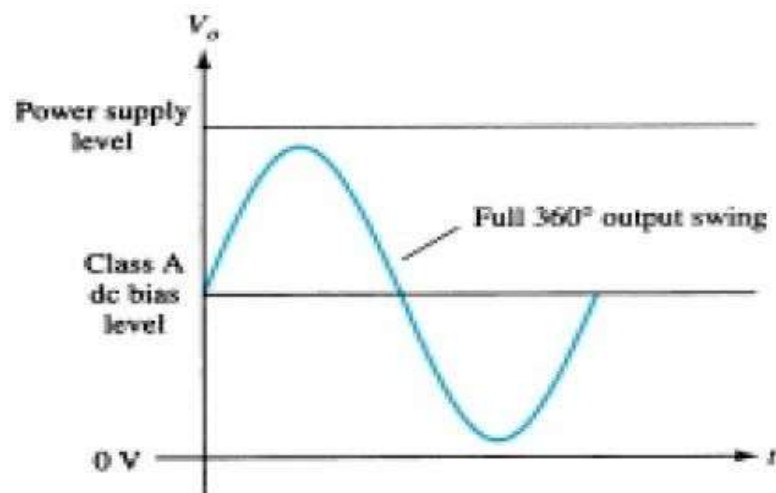
Fig. 9.1(a) Class A Amplifier

CLASS-B AMPLIFIER: A class B circuit provides an output signal varying over one-half the input signal cycle, or for 180° of signal, as shown in Fig. 9.1(b). The dc bias point for class B is therefore at 0 V, with the output then varying from this bias point for a half cycle. Obviously, the output is not a faithful reproduction of the input if only one half-cycle is present. Two class B operations—one to provide output on the positive output half-cycle and another

to provide operation on the negative-output half-cycle are necessary. The combined half-cycles then provide an output for a full 360° of operation. This type of connection is referred to as push-pull operation, which is discussed later in this chapter. Note that class B operation by itself creates a very distorted output signal since reproduction of the input takes place for only 180° of the output signal swing.
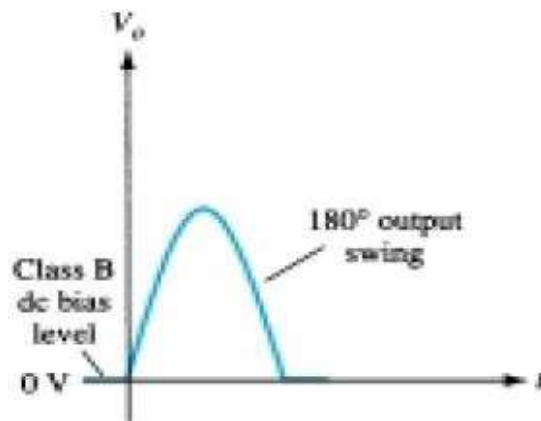
Fig. 9.1(b) Class B Amplifier

CLASS-AB AMPLIFIER: An amplifier may be biased at a dc level above the zero base current level of class B and above one-half the supply voltage level of class A; this bias condition is class AB. Class AB operation still requires a push-pull connection to achieve a full output cycle, but the dc bias level is usually closer to the zero base current level for better power efficiency, as described shortly. For class AB operation, the output signal swing occurs between 180° and 360° and is neither class A nor class B operation.

CLASS D AMPLIFIER: This operating class is a form of amplifier operation using pulse (digital) signals, which are on for a short interval and off for a longer interval. Using digital techniques makes it possible to obtain a signal that varies over the full cycle (using sample-and-hold circuitry) to recreate the output from many pieces of input signal.
The major advantage of class D operation is that the amplifier is on (using power) only for short intervals and the overall efficiency can practically be very high.

I.   SERIES-FED CLASS A AMPLIFIER

The simple fixed-bias circuit connection shown in Fig. 9.2 can be used to discuss the main features of a class A series-fed amplifier. The only differences between this circuit and the small-signal version considered previously is that the signals handled by the large-signal circuit are in the range of volts and the transistor used is a power transistor that is capable of operating in the range of a

few to tens of watts. As will be shown in this section, this circuit is not the best to use as a large-signal amplifier because of its poor power efficiency. The beta of a power transistor is generally less than 100, the overall amplifier circuit using power transistors that are capable of handling large power or current while not providing much voltage gain.
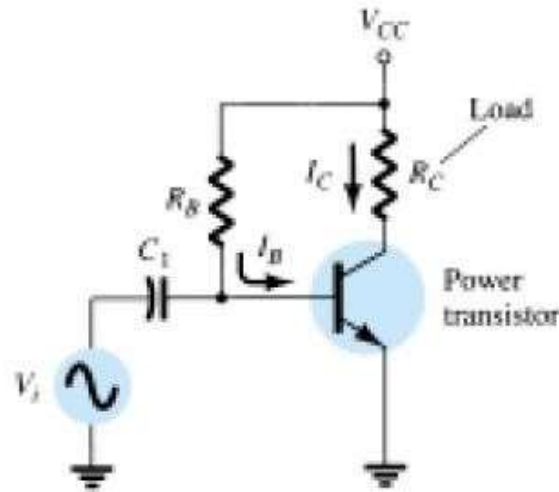
Fig. 9.2 Series-fed class A large-signal amplifier

DC Bias Operation :

The dc bias set by V_{CC} and R_B fixes the dc base-bias current at
$I_B = (V_{CC} - 0.7V) / R_B$ ------------- (9.1)
with the collector current then being
$I_C = \beta I_B$ ------------------------------- (9.2)
with the collector–emitter voltage then
$V_{CE} = V_{CC} - I_C R_C$ --------------------- (9.3)

To appreciate the importance of the dc bias on the operation of the power amplifier, consider the collector characteristic shown in Fig. 9.3. An ac load line is drawn using the values of *VCC* and *RC*. The intersection of the dc bias value of *IB* with the dc load line then determines the operating point (*Q*-point) for the circuit. The quiescent point values are those calculated using Eqs. (9.1) through (9.3). If the dc bias collector current is set at one-half the possible signal swing (between 0 and *VCC/RC*), the largest collector current swing will be possible. Additionally, if the quiescent collector–emitter voltage is set at one-half the supply voltage, the largest voltage swing will be possible. With the *Q*-point set at this optimum bias point, the power considerations for the circuit of Fig. 9.2 are determined as described below.
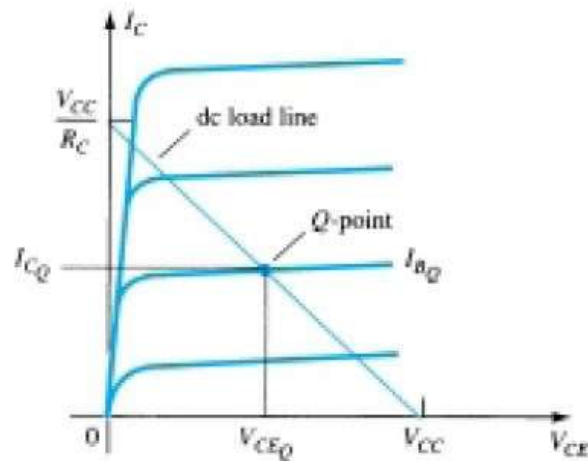
Fig. 9.3 Transistor characteristic showing load line and Q-point

AC Operation:

When an input ac signal is applied to the amplifier of Fig. 9.2, the output will vary from its dc bias operating voltage and current. A small input signal, as shown in Fig. 9.4, will cause the base current to vary above and below the dc bias point, which will then cause the collector current (output) to vary from the dc bias point set as well as the collector–emitter voltage to vary around its dc bias value. As the input signal is made larger, the output will vary further around the established dc bias point until either the current or the voltage reaches a limiting condition. For the current this limiting condition is either zero current at the low end or V_{CC}/R_C at the high end of its swing. For the collector–emitter voltage, the limit is either 0 V or the supply voltage, V_{CC}.
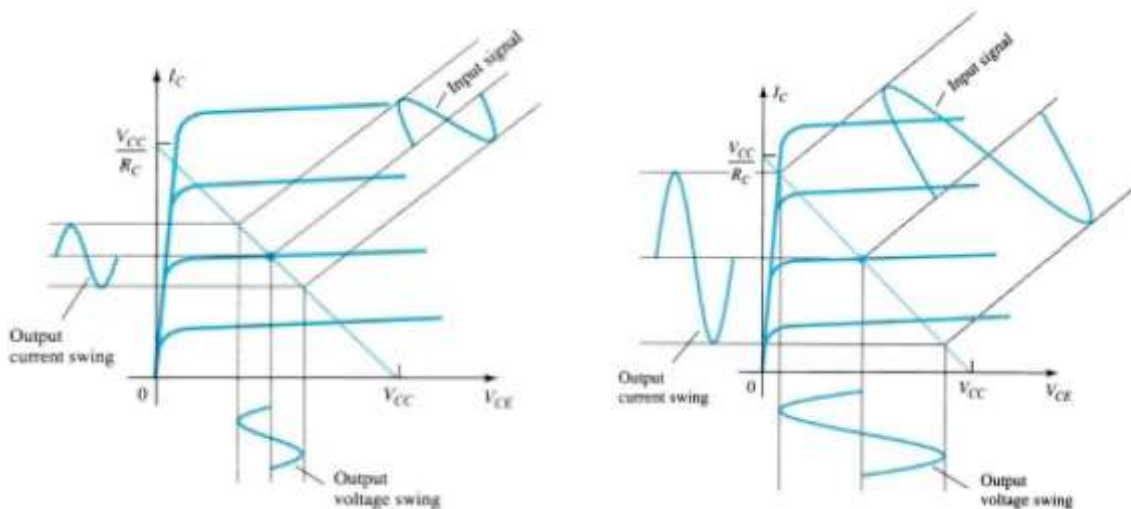
Fig. 9.4 Amplifier input and output signal variation

Power Considerations

The power into an amplifier is provided by the supply. With no input signal, the dc current drawn is the collector bias current, I_{CQ}. The power then drawn from the supply is

$$P_i(dc) = V_{CC}I_{CQ} \text{ -------------(9.4)}$$

Even with an ac signal applied, the average current drawn from the supply remains the same, so that Eq. (9.4) represents the input power supplied to the class A series-fed amplifier.

OUTPUT POWER

The output voltage and current varying around the bias point provide ac power to the load. This ac power is delivered to the load, R_C, in the circuit of Fig. 9.2. The ac signal, V_i, causes the base current to vary around the dc bias current and the collector current around its quiescent level, I_{CQ}. As shown in Fig. 9.4, the ac input signal results in ac current and ac voltage signals. The larger the input signal, the larger the output swing, up to the maximum set by the circuit. The ac power delivered to the load (R_C) can be expressed in a number of ways.

Using rms signals: The ac power delivered to the load (R_C) may be expressed using

$$P_O(ac) = V_{CE}(rms)I_C(rms) \text{ ---------------------------- (9.5a)}$$
$$P_O(ac) = I^2_C(rms)R_C \text{ ----------------------------------- (9.5b)}$$
$$P_O(ac) = V^2_C(rms)/R_C \text{ --------------------------------- (9.5c)}$$

**Using peak signals:** The ac power delivered to the load may be expressed using

$$P_O(ac) = V_{CE}(p)I_C(p)/2 \text{ --------------------------------- (9.6a)}$$
$$P_O(ac) = I^2_C(p)/R_C \text{ -------------------------------------- (9.6b)}$$
$$P_O(ac) = V^2_{CE}(p)/2R_C \text{ ----------------------------------(9.6c)}$$

Using peak-to-peak signals: The ac power delivered to the load may be expressed using

$$P_O(ac) = V_{CE}(p\text{-}p)I_C(p\text{-}p)/8 \text{ ----------------------------------- (9.7a)}$$
$$P_O(ac) = I^2_C(p\text{-}p)/8R_C \text{ -- (9.7b)}$$
$$P_O(ac) = V^2_{CE}(p\text{-}p)/8R_C \text{ -------------------------------------- (9.7c)}$$

Efficiency

The efficiency of an amplifier represents the amount of ac power delivered (transferred) from the dc source. The efficiency of the amplifier is calculated using

$$\%\eta = P_O(ac)/P_i(dc) \times 100\% \text{ --- (9.8)}$$

MAXIMUM EFFICIENCY

For the class A series-fed amplifier, the maximum efficiency can be determined using the maximum voltage and current swings. For the voltage swing it is
maximum V_{CE}(p-p) $= V_{CC}$
For the current swing it is
maximum I_C(p-p) $= V_{CC}/R_C$
Using the maximum voltage swing in Eq. (9.7a) yields
maximum Po(ac) $= V_{CC}(V_{CC}/R_C)/8 = V^2_{CC}/8R_C$
The maximum power input can be calculated using the dc bias current set to one-half the maximum value:
maximum P_i(dc) $= V_{CC}$(maximum I_C)$= V_{CC}(V_{CC}R_C)/2 = V^2_{CC}/2R_C$
We can then use Eq. (9.8) to calculate the maximum efficiency:
maximum % η = maximum P_O(ac)/maximum P_i(dc)x100%
$$= (V^2_{CC}/8R_C)/(V^2_{CC}/2R_C)x100\% = 25\%$$

The maximum efficiency of a class A series-fed amplifier is thus seen to be 25%. Since this maximum efficiency will occur only for ideal conditions of both voltage swing and current swing, most series-fed circuits will provide efficiencies of much less than 25%.

9.2 TRANSFORMER-COUPLED CLASS A AMPLIFIER

A form of class A amplifier having maximum efficiency of 50% uses a transformer to couple the output signal to the load as shown in Fig. 9.6. This is a simple circuit form to use in presenting a few basic concepts. Since the circuit uses a transformer to step voltage or current, a review of voltage and current step-up and step-down is presented.
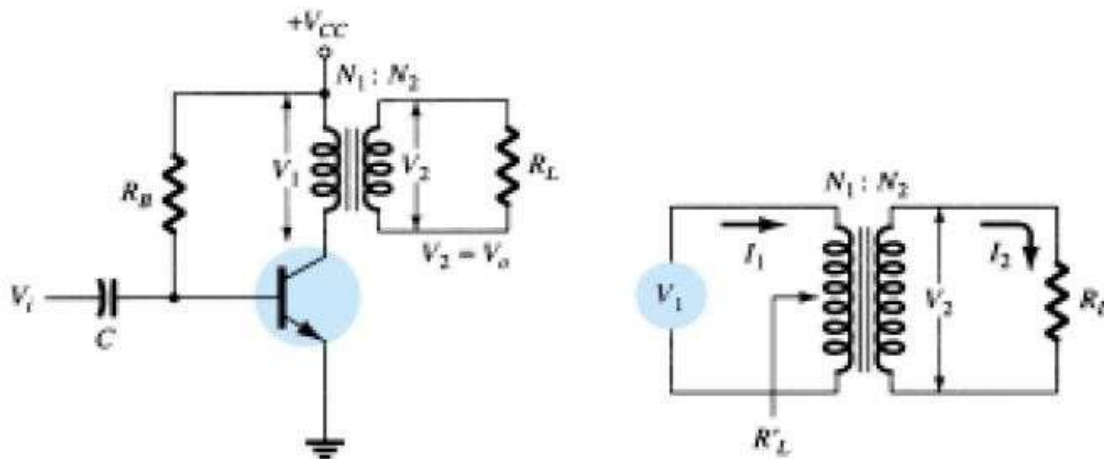
Fig 9.6: Transformer-coupled audio power amplifier

Transformer Action

A transformer can increase or decrease voltage or current levels according to the turns ratio, as explained below. In addition, the impedance connected to one side of a transformer can be made to appear either larger or smaller (step up or step down) at the other side of the transformer, depending on the square of the transformer winding turns ratio. The following discussion assumes ideal (100%) power transfer from primary to secondary, that is, no power losses are considered.

VOLTAGE TRANSFORMATION

As shown in Fig. 9.7a, the transformer can step up or step down a voltage applied to one side directly as the ratio of the turns (or number of windings) on each side. The voltage transformation is given by
$V_2/V_1 = N_2/N_1$ --------------------------------------- (9.9)
Equation (9.9) shows that if the number of turns of wire on the secondary side is larger than on the primary, the voltage at the secondary side is larger than the voltage at the primary side.

CURRENT TRANSFORMATION

The current in the secondary winding is inversely proportional to the number of turns in the windings. The current transformation is given by
$I_2/I_1 = N_1/N_2$ ---------------------------------------(9.10)

Fig 9.7 Transformer operation: (a) voltage transformation; (b) current transformation; (c) impedance transformation.

This relationship is shown in Fig. 9.7b. If the number of turns of wire on the secondary is greater than that on the primary, the secondary current will be less than the current in the primary.

IMPEDANCE TRANSFORMATION

Since the voltage and current can be changed by a transformer, an impedance seen from either side (primary or secondary) can also be changed. As shown in Fig. 9.7c, an impedan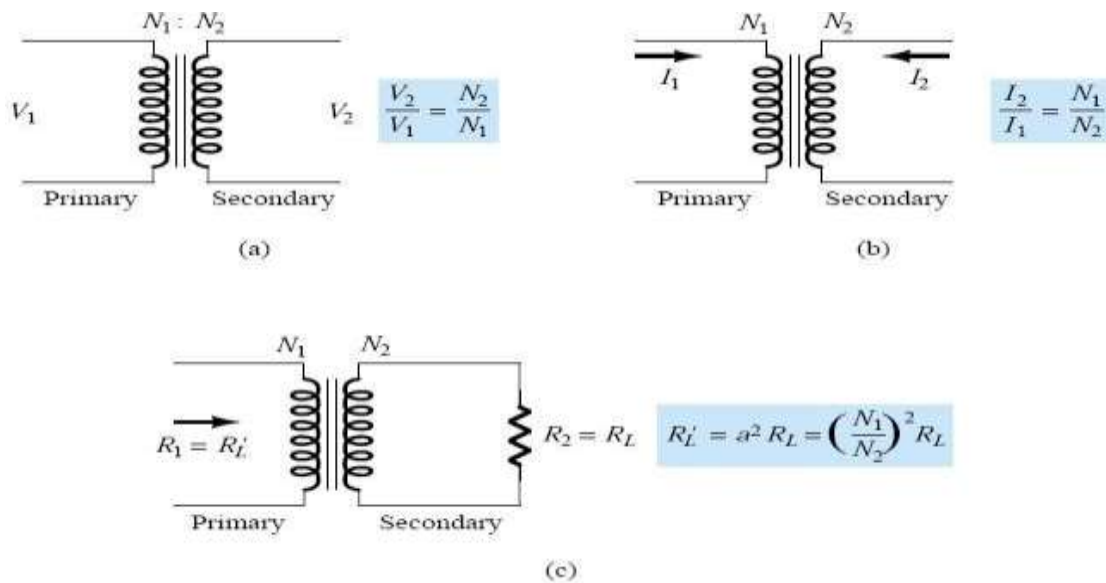ce R_L is connected across the transformer secondary. This impedance is changed by the transformer when viewed at the primary side (R'_L). This can be shown as follows:
$R_L/R'_L = R_2/R_1 = (N_2/N_1)^2$
If we define a $=N_1/N_2$, where a is the turns ratio of the transformer, the above equation becomes,
$R'_L/R_L = R_1/R_2 = (N_1/N_2)^2 = a^2$ ------------------------------------(9.11)
We can express the load resistance reflected to the primary side as:
$R_1 = a^2R_2$ or $R'_L = a^2R_L$ ---------------------------------------(9.12)
where R'_L is the reflected impedance. As shown in Eq. (9.12), the reflected impedance is related directly to the square of the turns ratio. If the number of turns of the secondary is smaller than that of the primary, the impedance seen looking into the primary is larger than that of the secondary by the square of the turns ratio.

Operation of Amplifier Stage

DC LOAD LINE

The transformer (dc) winding resistance determines the dc load line for the circuit of Fig. 9.6. Typically, this dc resistance is small (ideally 0Ω) and, as shown in Fig. 9.8, a 0-Ω dc load line is a straight vertical line. A practical transformer winding resistance would be a few ohms, but only the ideal case will be considered in this discussion. There is no dc voltage drop across the 0-Ω dc load resistance, and the load line is drawn straight vertically from the voltage point, $V_{CEQ} =V_{CC}$.
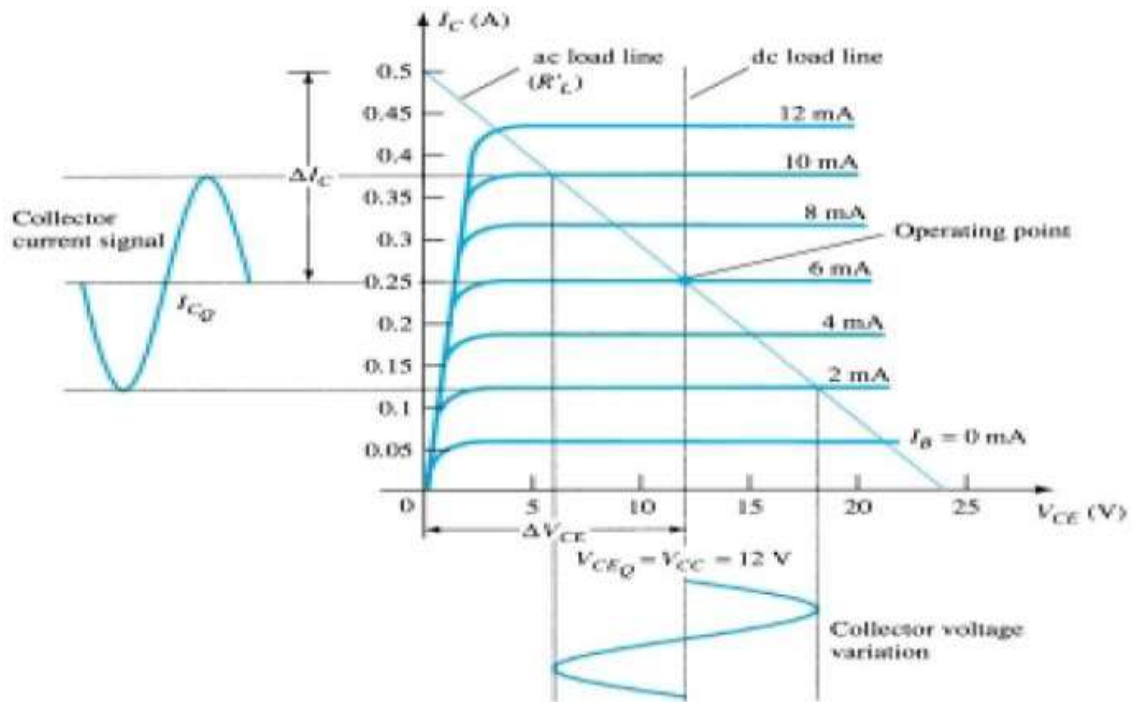
Fig 9.8 Load lines for class A transformer-coupled amplifier

QUIESCENT OPERATING POINT

The operating point in the characteristic curve of Fig. 9.8 can be obtained graphically at the point of intersection of the dc load line and the base current set by the circuit. The collector quiescent current can then be obtained from the operating point. In class A operation, keep in mind that the dc bias point sets the conditions for the maximum undistorted signal swing for both collector current and collector–emitter voltage. If the input signal produces a voltage swing less than the maximum possible, the efficiency of the circuit at that time will be less than 25%. The dc bias point is therefore important in setting the operation of a class A series-fed amplifier.

AC LOAD LINE

To carry out ac analysis, it is necessary to calculate the ac load resistance "seen" looking into the primary side of the transformer, then draw the ac load line on the collector characteristic. The reflected load resistance (R'L) is calculated using Eq. (9.12) using the value of the load connected across the secondary (R$_L$) and the turns ratio of the transformer. The graphical analysis technique then proceeds as follows. Draw the ac load line so that it passes through the operating point and has a slope equal to -1/R'$_L$ (the reflected load resistance), the load line slope being the negative reciprocal of the ac load resistance. Notice that the ac load line shows that the output signal swing can exceed the value of V$_{CC}$. In fact, the voltage developed across

the transformer primary can be quite large. It is therefore necessary after obtaining the ac load line to check that the possible voltage swing does not exceed transistor maximum ratings.

SIGNAL SWING AND OUTPUT AC POWER

Fig 9.9 shows the voltage and current signal swings from the circuit of Fig. 9.6. From the signal variations shown in Fig. 9.9, the values of the peak-to-peak signal swings are

$$V_{CE}(p\text{-}p) = V_{CE}\,max - V_{CE}\,min$$
$$I_C(p\text{-}p) = I_C\,max - I_C\,min$$

The ac power developed across the transformer primary can then be calculated using

$$P_O(ac) = [(V_{CE}\,max - V_{CE}\,min)(I_C\,max - I_C\,min)]/8 \text{------------ (9.13)}$$

The ac power calculated is that developed across the primary of the transformer. Assuming an ideal transformer (a highly efficient transformer has an efficiency of well over 90%), the power delivered by the secondary to the load is approximately that calculated using Eq. (9.13). The output ac power can also be determined using the voltage delivered to the load.
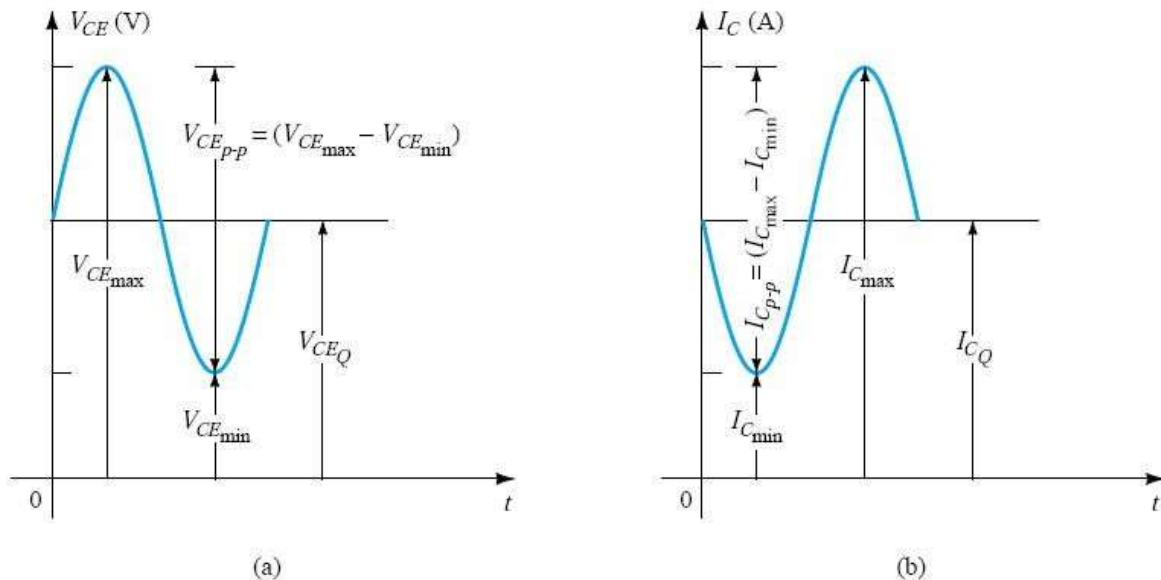

Fig 9.9: Graphical operation of transformer-coupled class A amplifier

For the ideal transformer, the voltage delivered to the load can be calculated using Eq. (9.9):
$$V_L = V_2 = (N_2/N_1)V_1$$
The power across the load can then be expressed as
$$P_L = V^2{}_L(rms)/R_L$$

and equals the power calculated using Eq. (9.5c).
Using Eq. (9.10) to calculate the load current yields
$I_L = I_2 = (N_1/N_2)I_C$
with the output ac power then calculated using
$P_L = I^2_L(rms)R_L$

Efficiency

So far we have considered calculating the ac power delivered to the load. We next consider the input power from the battery, power losses in the amplifier, and the overall power efficiency of the transformer-coupled class A amplifier. The input (dc) power obtained from the supply is calculated from the supply dc voltage and the average power drawn from the supply:

$$P_i(dc) = V_{CC}I_{CQ}$$

For the transformer-coupled amplifier, the power dissipated by the transformer is small (due to the small dc resistance of a coil) and will be ignored in the present calculations. Thus the only power loss considered here is that dissipated by the power transistor and calculated using

$$P_Q = P_i(dc) - P_i(ac)$$

where P_Q is the power dissipated as heat. While the equation is simple, it is nevertheless significant when operating a class A amplifier. The amount of power dissipated by the transistor is the difference between that drawn from the dc supply (set by the bias point) and the amount delivered to the ac load. When the input signal is very small, with very little ac power delivered to the load, the maximum power is dissipated by the transistor. When the input signal is larger and power delivered to the load is larger, less power is dissipated by the transistor. In other words, the transistor of a class A amplifier has to work hardest (dissipate the most power) when the load is disconnected from the amplifier, and the transistor dissipates least power when the load is drawing maximum power from the circuit.

MAXIMUM THEORETICAL EFFICIENCY

For a class A transformer-coupled amplifier, the maximum theoretical efficiency goes up to 50%. Based on the signals obtained using the amplifier, the efficiency can be expressed as

$$\%\eta = 50[(V_{CEmax} - V_{CEmin})/(V_{CEmax} + V_{CEmin})]^2 \%$$

The larger the value of V_{CEmax} and the smaller the value of V_{CEmin}, the closer the efficiency approaches the theoretical limit of 50%.

9.3 CLASS B AMPLIFIER OPERATION

Class B operation is provided when the dc bias leaves the transistor biased just off, the transistor turning on when the ac signal is applied. This is essentially no bias, and the transistor conducts current for only one-half of the signal cycle. To obtain output for the full cycle of signal, it is necessary to use two transistors and have each conduct on opposite half-cycles, the combined operation providing a full cycle of output signal. Since one part of the circuit pushes the signal high during one half-cycle and the other part pulls the signal low during the other half-cycle, the circuit is referred to as a *push-pull circuit.* Fig 9.12 shows a diagram for push-pull operation. An ac input signal is applied to the push-pull circuit, with each half operating on alternate half-cycles, the load then receiving a signal for the full ac cycle. The power transistors used in the push-pull circuit are capable of delivering the desired power to the load, and the class B operation of these transistors provides greater efficiency than was possible using a single transistor in class A operation.
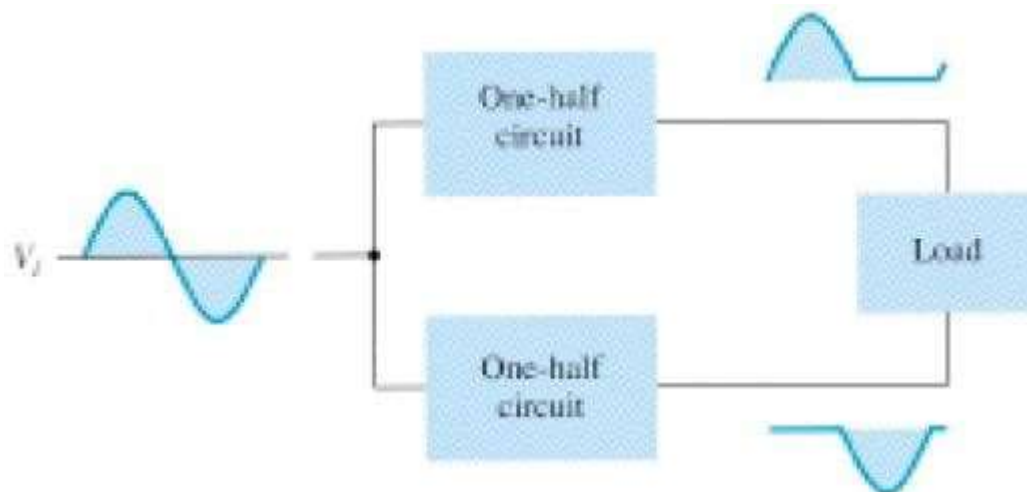
Fig. 9.12 Block representation of push-pull operation

Input (DC) Power

The power supplied to the load by an amplifier is drawn from the power supply (or power supplies; Fig. 9.13) that provides the input or dc power. The amount of this input power can be calculated using

$P_i(dc) = V_{CC}I_{dc}$ ------------------------------------- (9.17)

where I_{dc} is the average or dc current drawn from the power supplies. In class B operation, the current drawn from a single power supply has the form of a full-wave rectified signal, while that drawn from two power supplies has the form of a half-wave rectified signal from each supply.
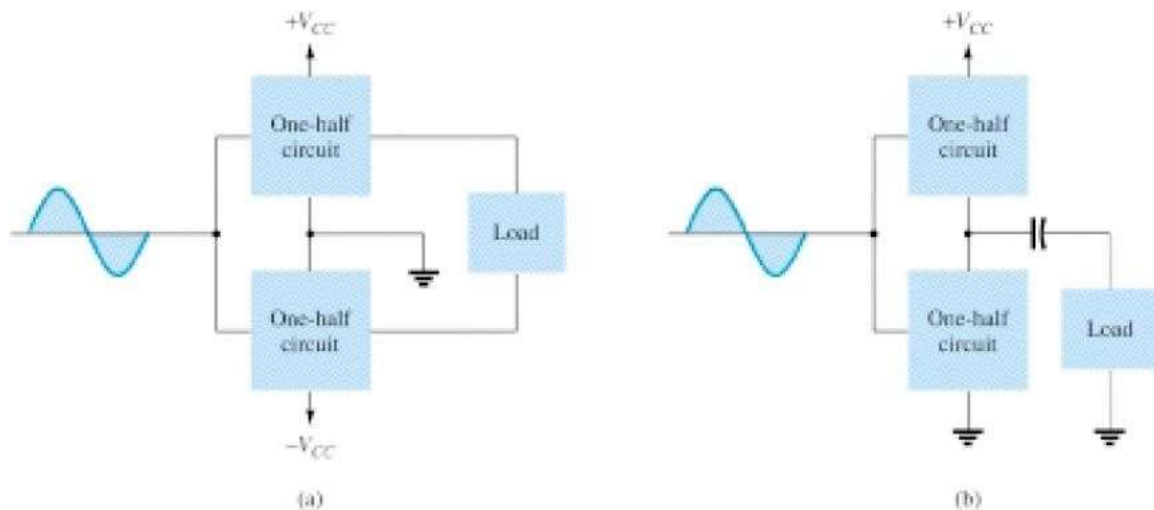
Fig 9.13 Connection of push-pull amplifier to load: (a) using two voltage supplies; (b) using one voltage supply

In either case, the value of the average current drawn can be expressed as

$I_{dc} = (2/\pi)I(p)$ -------------------------------- (9.18)

where I(p) is the peak value of the output current waveform. Using Eq. (9.18) in the power input equation (Eq. 9.17) results in

$P_i(dc) = V_{CC}((2/\pi)I(p))$ ------------------- (9.19)

Output (AC) Power

The power delivered to the load (usually referred to as a resistance, R_L) can be calculated using any one of a number of equations. If one is using an rms meter to measure the voltage across the load, the output power can be calculated as

$P_O(ac) = V^2_L(rms)/R_L$ ----------------------- (9.20)

If one is using an oscilloscope, the peak, or peak-to-peak, output voltage measured can be used:

$P_O(ac) = V^2_L(p\text{-}p)/8R_L = V^2_L(p)/2R_L$ ------------ (9.21)

The larger the rms or peak output voltage, the larger the power delivered to the load.

Efficiency

The efficiency of the class B amplifier can be calculated using the basic equation:

$\%\eta = P_O(ac)/P_O(dc)x100\%$

Using Eqs. (9.19) and (9.21) in the efficiency equation above results in

$\%\eta = P_O(ac)/P_O(dc) \times 100\% = [V_L^2(p)/2R_L]/V_{CC}[(2/\pi)I(p)]$

$\quad = (\pi/4) \times V_L(p)/V_{CC} \times 100\%$ ---------------------------- (9.22)

(using $I(p) = V_L(p)/R_L$). Equation (9.22) shows that the larger the peak voltage, the higher the circuit efficiency, up to a maximum value when $V_L(p) = V_{CC}$, this maximum efficiency then being

maximum efficiency = $(\pi/4) \times 100\% = 78.5\%$

Power Dissipated by Output Transistors

The power dissipated (as heat) by the output power transistors is the difference between the input power delivered by the supplies and the output power delivered to the load.

$\qquad P_{2Q} = P_i(dc) - P_i(ac)$ ---------------------------- (9.23)

where P_{2Q} is the power dissipated by the two output power transistors. The dissipated power handled by each transistor is then

$\qquad P_Q = P_{2Q}/2$ ----------------------------------- (9.24)

Maximum Power Considerations

For class B operation, the maximum output power is delivered to the load when $V_L(p) = V_{CC}$.

$\qquad$ Maximum $P_O(ac) = V_{CC}^2/2R_L$ ---------------- (9.25)

The corresponding peak ac current $I(p)$ is then

$I(p) = V_{CC}^2/R_L$

so that the maximum value of average current from the power supply is

maximum $I_{dc} = (2/\pi)I(p) = 2V_{CC}/\pi R_L$

Using this current to calculate the maximum value of input power results in

Maximum $P_i(dc) = V_{CC}(\text{maximum } I_{dc}) = V_{CC}(2V_{CC}/\pi R_L) = 2V_{CC}^2/\pi R_L$ --- (9.26)

The maximum circuit efficiency for class B operation is then

Maximum $\%\eta = P_O(ac)/P_i(dc) \times 100\% = [V_{CC}^2/2R_L]/[2V_{CC}^2/\pi R_L] \times 100\%$

$\qquad\qquad = (\pi/4) \times 100\% = 78.54\%$ ------------------------- (9.27)

When the input signal results in less than the maximum output signal swing, the circuit efficiency is less than 78.5%.

For class B operation, the maximum power dissipated by the output transistors does not occur at the maximum power input or output condition. The maximum power dissipated by the two output transistors occurs when the output voltage across the load is

$VL(p) = 0.636 VCC = (2/\pi)VCC$

for a maximum transistor power dissipation of

maximum $P_{2Q} = 2V_{CC}^2/\pi^2 R_L$ -------------------------------------(9.28)

The maximum efficiency of a class B amplifier can also be expressed as follows:

$P_O(ac) = V^2_L(p)/2R_L$

$P_i(ac) = V_{CC}I_{dc} = V_{CC}[2V_L(p)/\pi R_L]$

So that

$\%\eta = P_O(ac) / P_i(ac) \times 100\% = [V^2_L(p)/2R_L]/ V_{CC}[2V_L(p)/\pi R_L] \times 100\%$

$= 78.54V_L(p)/V_{CC}\%$ -------------------------------- (9.29)

9.4 CLASS B AMPLIFIER CIRCUITS

A number of circuit arrangements for obtaining class B operation are possible. We will consider the advantages and disadvantages of a number of the more popular circuits in this section. The input signals to the amplifier could be a single signal, the circuit then providing two different output stages, each operating for one-half the cycle. If the input is in the form of two opposite polarity signals, two similar stages could be used, each operating on the alternate cycle because of the input signal. One means of obtaining polarity or phase inversion is using a transformer, the transformer-coupled amplifier having been very popular for a long time. Opposite polarity inputs can easily be obtained using an op-amp having two opposite outputs or using a few op-amp stages to obtain two opposite polarity signals. An opposite polarity operation can also be achieved using a single input and complementary transistors (*npn* and *pnp*, or *n*MOS and *p*MOS).

Fig 9.14 shows different ways to obtain phase-inverted signals from a single input signal. Figure 16.14a shows a center-tapped transformer to provide opposite phase signals. If the transformer is exactly center-tapped, the two signals are exactly opposite in phase and of the same magnitude. The circuit of Fig. 9.14b uses a BJT stage with in-phase output from the emitter and opposite phase output from the collector. If the gain is made nearly 1 for each output, the same magnitude results. Probably most common would be using op-amp stages, one to provide an inverting gain of unity and the other a non-inverting gain of unity, to provide two outputs of the same magnitude but of opposite phase.
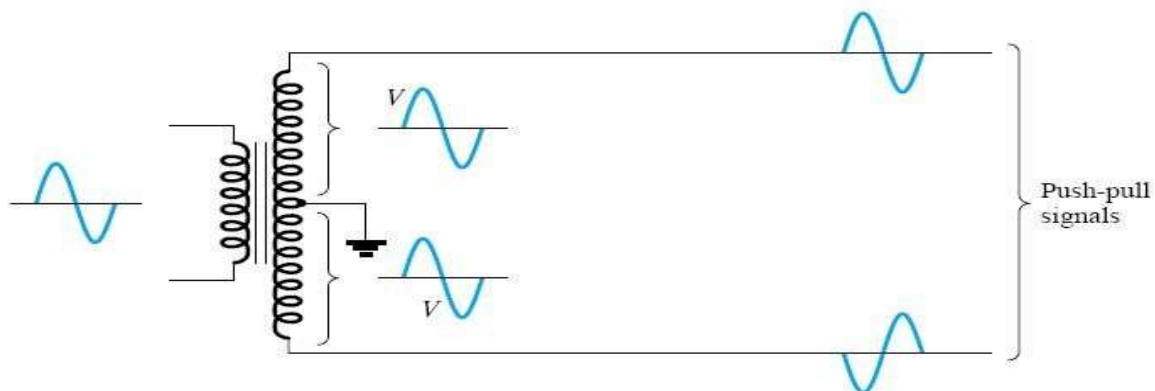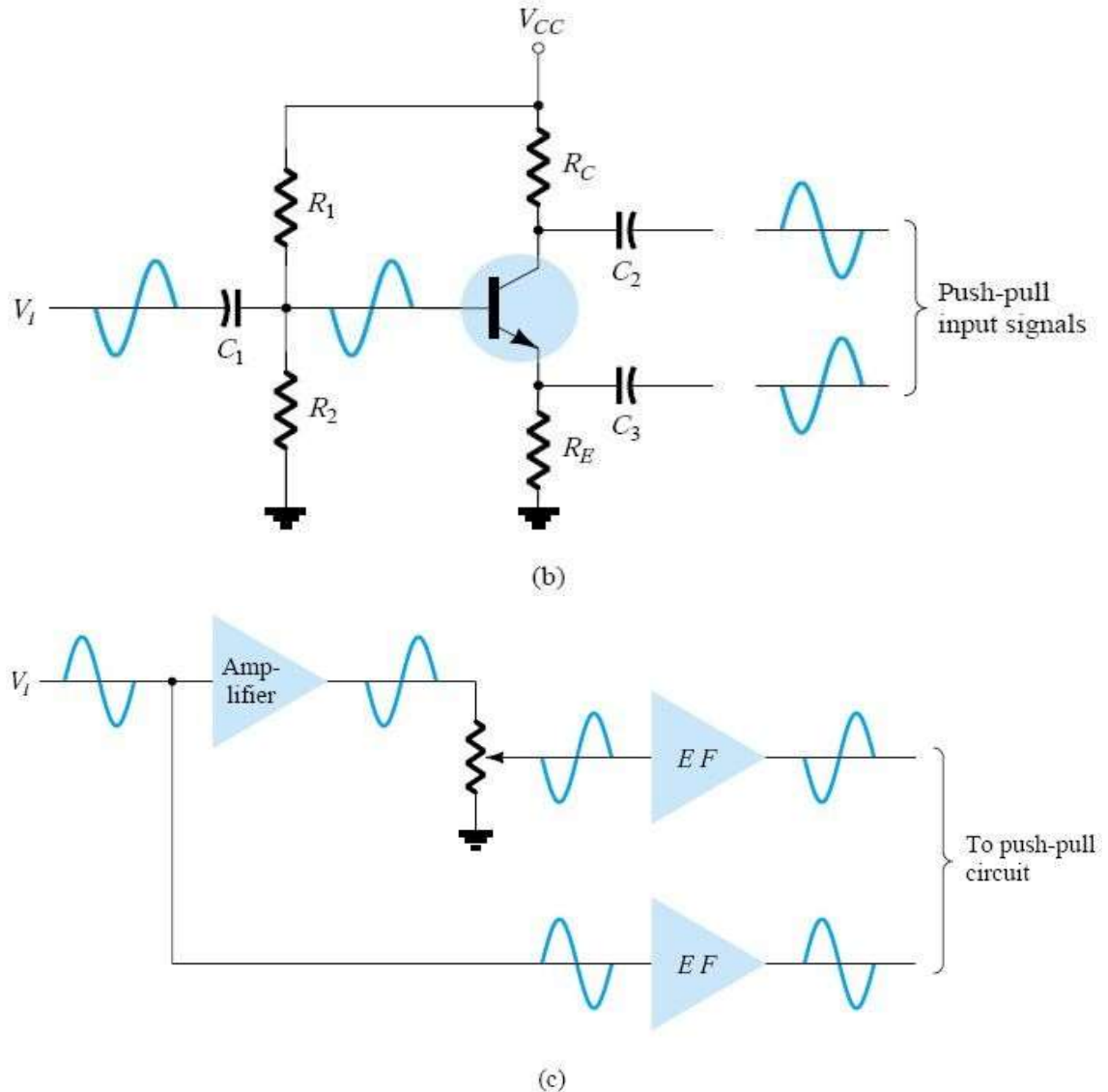

(a)

Fig. 9.14 Phase Splitter Circuits

9.5 TRANSFORMER-COUPLED PUSH–PULL CIRCUITS

The circuit of Fig. 9.15 uses a center-tapped input transformer to produce opposite polarity signals to the two transistor inputs and an output transformer to drive the load in a push-pull mode of operation described next.
During the first half-cycle of operation, transistor Q1 is driven into conduction whereas transistor Q2 is driven off. The current I1 through the transformer results in the first half-cycle of signal to the load. During the second half-cycle of the input signal, Q2 conducts whereas Q1 stays off, the current I2 through the transformer resulting in the second half-cycle to the load. The overall signal developed across the load then varies over the full cycle of signal operation.
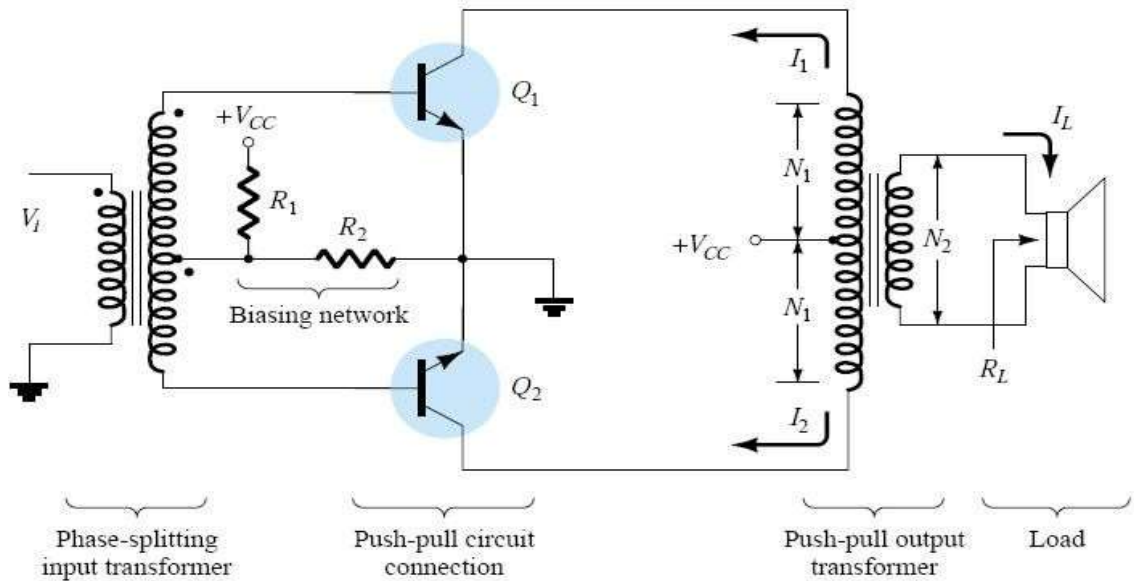
Fig.9.15 Push-Pull Circuit

9.6 COMPLEMENTARY-SYMMETRY CIRCUITS

Using complementary transistors (*npn and pnp*) it is possible to obtain a full cycle output across a load using half-cycles of operation from each transistor, as shown in Fig. 9.16a. While a single input signal is applied to the base of both transistors, the transistors, being of opposite type, will conduct on opposite half-cycles of the input.

The *npn* transistor will be biased into conduction by the positive half-cycle of signal, with a resulting half-cycle of signal across the load as shown in Fig. 9.16b. During the negative half-cycle of signal, the *pnp* transistor is biased into conduction when the input goes negative, as shown in Fig. 9.16c.

During a complete cycle of the input, a complete cycle of output signal is developed across the load. One disadvantage of the circuit is the need for two separate voltage supplies. Another, less obvious disadvantage with the complementary circuit is shown in the resulting crossover distortion in the output signal (see Fig. 9.16d).

Crossover distortion refers to the fact that during the signal crossover from positive to negative (or vice versa) there is some nonlinearity in the output signal. This results from the fact that the circuit does not provide exact switching of one transistor off and the other on at the zero-voltage condition. Both transistors may be partially off so that the output voltage does not follow the input around the zero-voltage condition.

Biasing the transistors in class AB improves this operation by biasing both transistors to be on for more than half a cycle.
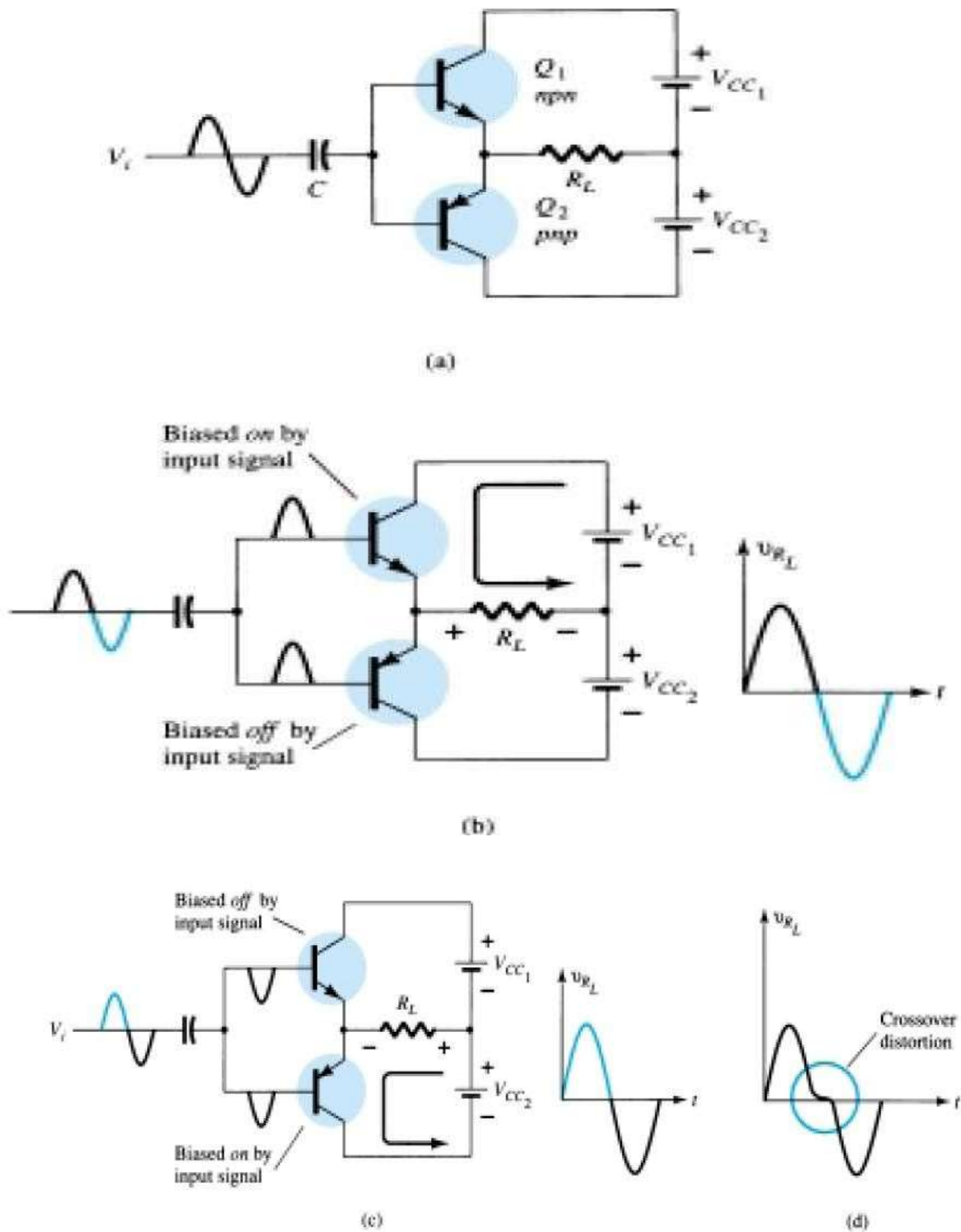
Fig. 9.16 Complementary-symmetry push-pull circuit

A more practical version of a push-pull circuit using complementary transistors is shown in Fig. 9.17. Note that the load is driven as the output of an emitter follower so that the load resistance of the load is matched by the low output resistance of the driving source. The circuit uses complementary Darlington-

connected transistors to provide higher output current and lower output resistance.
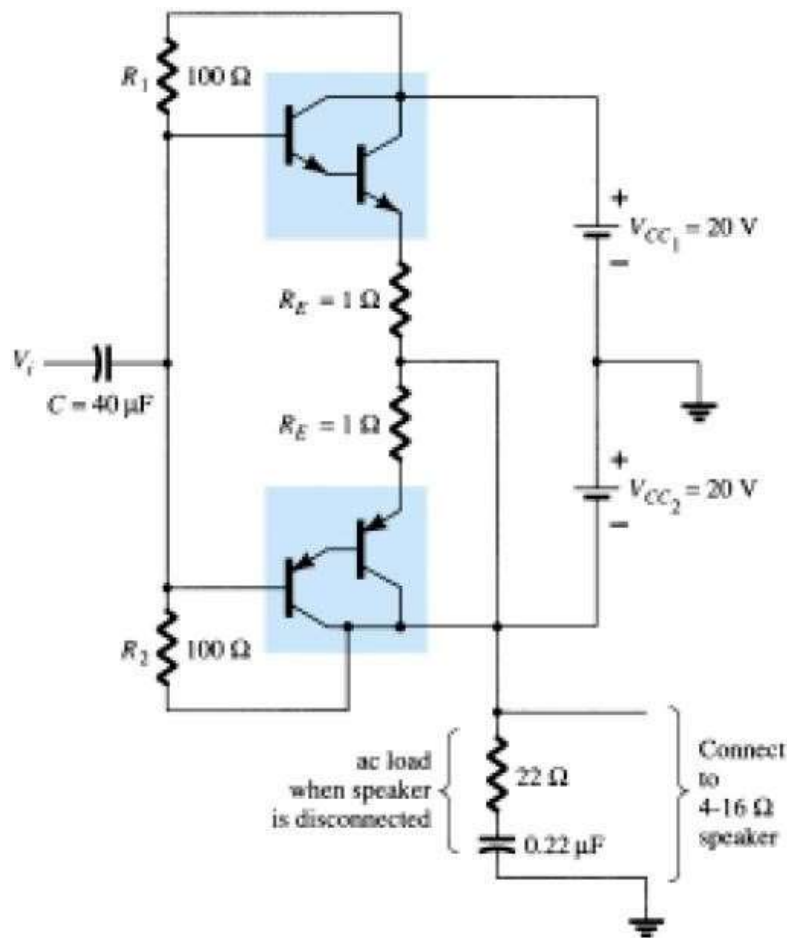

Fig. 9.17 Complementary symmetry push-pull circuit using Darlington
transistors

9.7 QUASI-COMPLEMENTARY PUSH–PULL AMPLIFIER

In practical power amplifier circuits, it is preferable to use *npn* transistors for both high-current-output devices. Since the push-pull connection requires complementary devices, a *pnp* high-power transistor must be used. A practical means of obtaining complementary operation while using the same, matched *npn* transistors for the output is provided by a quasi-complementary circuit, as shown in Fig. 9.18. The push- pull operation is achieved by using complementary transistors (*Q*1 and *Q*2) before the matched *npn* output transistors (*Q*3 and *Q*4). Notice that transistors *Q*1 and *Q*3 form a Darlington connection that provides output from a low-impedance emitter-follower.

The connection of transistors $Q2$ and $Q4$ forms a feedback pair, which similarly provides a low-impedance drive to the load. Resistor $R2$ can be adjusted to minimize crossover distortion by adjusting the dc bias condition. The single input signal applied to the push-pull stage then results in a full cycle output to the load. The quasi-complementary push-pull amplifier is presently the most popular form of power amplifier.
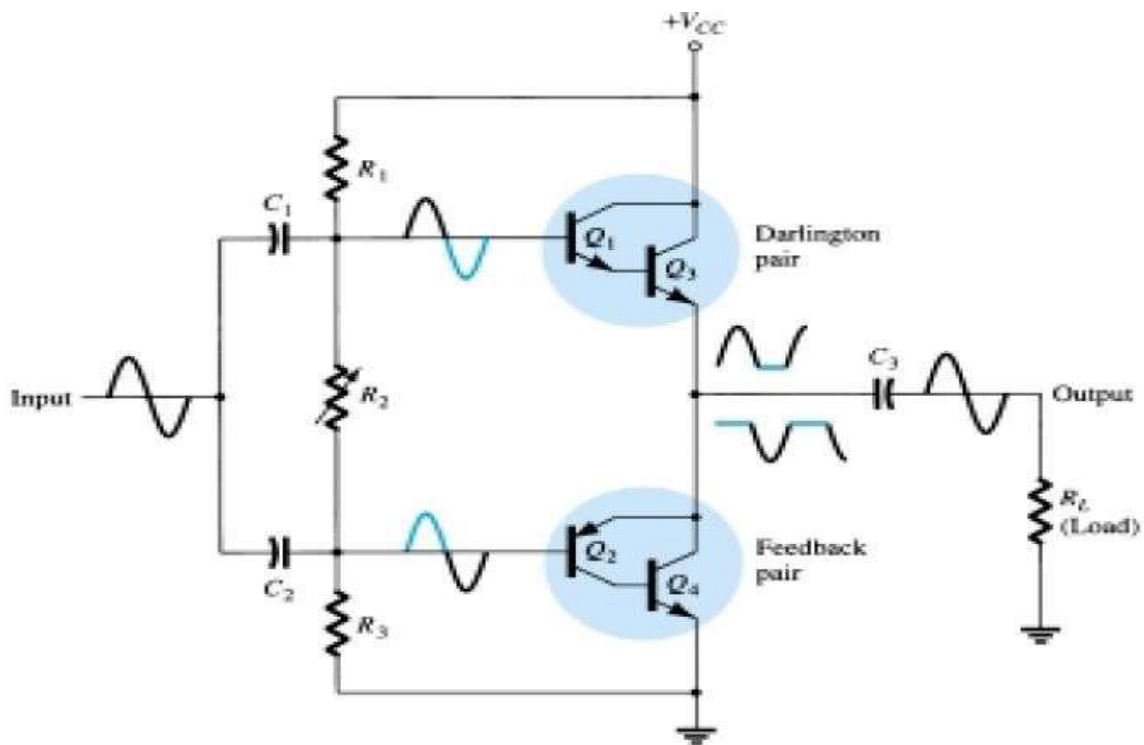

Fig. 9.18: Quasi-complementary push-pull transformerless power amplifier

9.8 AMPLIFIER DISTORTION

A pure sinusoidal signal has a single frequency at which the voltage varies positive and negative by equal amounts. Any signal varying over less than the full 360° cycle is considered to have distortion. An ideal amplifier is capable of amplifying a pure sinusoidal signal to provide a larger version, the resulting waveform being a pure single-frequency sinusoidal signal. When distortion occurs the output will not be an exact duplicate (except for magnitude) of the input signal.

Distortion can occur because the device characteristic is not linear, in which case nonlinear or amplitude distortion occurs. This can occur with all classes of amplifier operation. Distortion can also occur because the circuit elements and devices respond to the input signal differently at various frequencies, this being frequency distortion.

One technique for describing distorted but period waveforms uses Fourier analysis, a method that describes any periodic waveform in terms of its fundamental frequency component and frequency components at integer multiples—these components are called *harmonic components* or *harmonics.* For example, a signal that is originally 1000 Hz could result, after distortion, in a frequency component at 1000 Hz (1 kHz) and harmonic components at 2 kHz (2X1 kHz), 3 kHz (3X1 kHz), 4 kHz (4X1 kHz), and so on. The original frequency of 1 kHz is called the *fundamental frequency;* those at integer multiples are the harmonics. The 2-kHz component is therefore called a *second harmonic,* that at 3 kHz is the *third harmonic,* and so on. The fundamental frequency is not considered a harmonic. Fourier analysis does not allow for fractional harmonic frequencies—only integer multiples of the fundamental.

Harmonic Distortion

A signal is considered to have harmonic distortion when there are harmonic frequency components (not just the fundamental component). If the fundamental frequency has an amplitude, A_1, and the *n*th frequency component has an amplitude, A_n, a harmonic distortion can be defined as

% *n*th harmonic distortion = % $D_n = |A_n| / |A_1|$ x 100% ------------------- (9.30)

The fundamental component is typically larger than any harmonic component.

TOTAL HARMONIC DISTORTION

When an output signal has a number of individual harmonic distortion components, the signal can be seen to have a total harmonic distortion based on the individual elements as combined by the relationship of the following equation:

% THD = $(D_2^2 + D_3^2 + D_4^2 + \ldots)^{1/2}$ x100% --------------------- (9.31)

An instrument such as a spectrum analyzer would allow measurement of the harmonics present in the signal by providing a display of the fundamental component of a signal and a number of its harmonics on a display screen. Similarly, a wave analyzer instrument allows more precise measurement of the harmonic components of a distorted signal by filtering out each of these components and providing a reading of these components. In any case, the technique of considering any distorted signal as containing a fundamental component and harmonic components is practical and useful.

For a signal occurring in class AB or class B, the distortion may be mainly even harmonics, of which the second harmonic component is the largest. Thus, although the distorted signal theoretically contains all harmonic components from the second harmonic up, the most important in terms of the amount of distortion in the classes presented above is the second harmonic.

SECOND HARMONIC DISTORTION

Fig 9.20 shows a waveform to use for obtaining second harmonic distortion. A collector current waveform is shown with the quiescent, minimum, and maximum signal levels, and the time at which they occur is marked on the waveform. The signal shown indicates that some distortion is present.
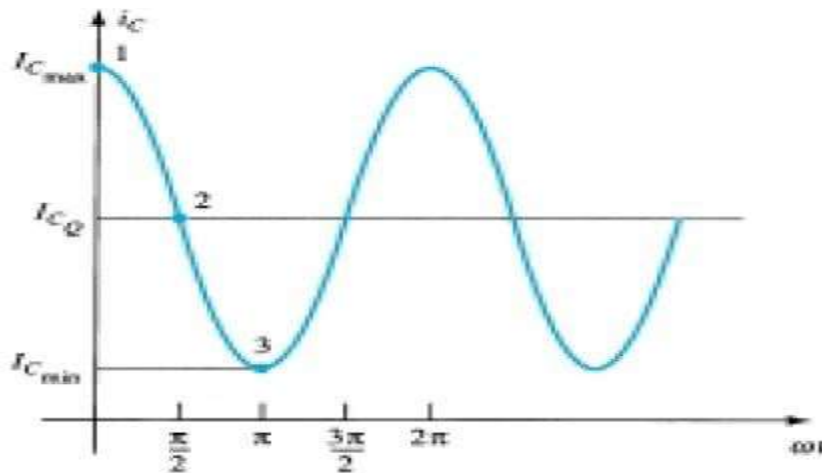

Fig. 9.20: Waveform for obtaining second harmonic distortion

An equation that approximately describes the distorted signal waveform is
$i_C = I_{CQ} + I_0 + I_1 \cos\omega t + I_2 \cos\omega t$ -----------------------(9.32)
the definition of second harmonic distortion may be expressed as
$D_2 = |I_2/I_1| \times 100\%$
$= [0.5(I_{Cmax}+I_{Cmin})-I_{CQ}]/[I_{Cmax}-I_{Cmin}] \times 100\%$ ---------- (9.33)
In a similar manner, the second harmonic distortion can be expressed in terms of measured collector–emitter voltages:
$D_2 = [0.5(V_{CEmax}+V_{CEmin})-V_{CEQ}]/[V_{CEmax}-V_{CEmin}] \times 100\%$ ---- (9.34)

Power of Signal Having Distortion

When distortion does occur, the output power calculated for the undistorted signal is no longer correct. When distortion is present, the output power delivered to the load resistor R_C due to the fundamental component of the distorted signal is
$P_1 = I_1^2 R_C/2$ ------------------------------- (9.35)
The total power due to all the harmonic components of the distorted signal can then be calculated using
$P1 = (I_1^2 + I_2^2 + I_3^2 + \ldots\ldots) \times R_C/2$ -------------------------- (9.36)
The total power can also be expressed in terms of the total harmonic distortion,
$P = (1 + D_2^2 + D_3^2 + \ldots\ldots) \times I_1^2 \times (R_C/2) = (1+THD^2)P_1$ -------------- (9.37)

9.9 CLASS C AND CLASS D AMPLIFIERS

Although class A, class AB, and class B amplifiers are most used as power amplifiers, class D amplifiers are popular because of their very high efficiency. Class C amplifiers, while not used as audio amplifiers, do find use in tuned circuits as used in communications.

Class C Amplifier

A class C amplifier, as that shown in Fig. 9.25, is biased to operate for less than 180° of the input signal cycle. The tuned circuit in the output, however, will provide a full cycle of output signal for the fundamental or resonant frequency of the tuned circuit (*L* and *C* tank circuit) of the output. This type of operation is therefore limited to use at one fixed frequency, as occurs in a communications circuit, for example. Operation of a class C circuit is not intended primarily for large-signal or power amplifiers.
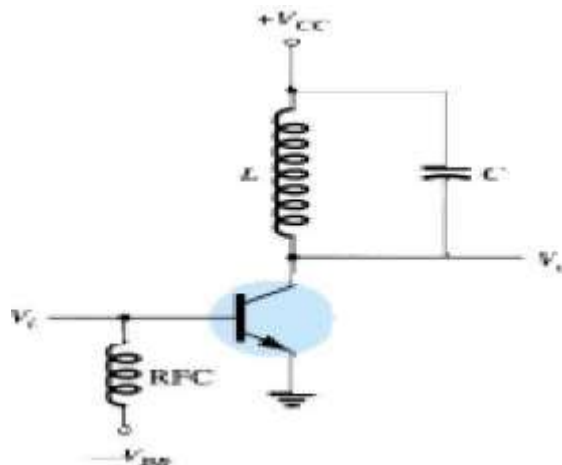

Fig. 9.25: Class C amplifier circuit

Class D Amplifier

A class D amplifier is designed to operate with digital or pulse-type signals. An efficiency of over 90% is achieved using this type of circuit, making it quite desirable in power amplifiers. It is necessary, however, to convert any input signal into a pulse type waveform before using it to drive a large power load and to convert the signal back to a sinusoidal-type signal to recover the original signal. A sinusoidal signal may be converted into a pulse-type signal using some form of sawtooth or chopping waveform to be applied with the input into a comparator type op-amp circuit so that a representative pulse-type signal is produced. While the letter D is used to describe the next type of bias operation after class C, the D could also be considered to stand for "Digital," since that is the nature of the signals provided to the class D amplifier.

Fig 9.26 shows a block diagram of the unit needed to amplify the class D signal and then convert back to the sinusoidal-type signal using a low-pass filter. Since the amplifier's transistor devices used to provide the output are basically either off or on, they provide current only when they are turned on, with little power loss due to their low on-voltage. Since most of the power applied to the amplifier is transferred to the load, the efficiency of the circuit is typically very high. Power MOSFET devices have been quite popular as the driver devices for the class D amplifier.
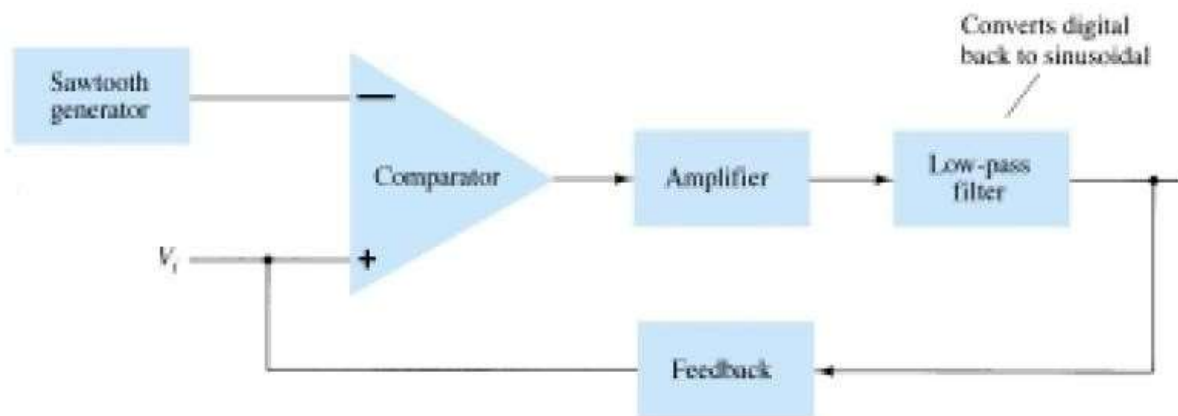

Fig. 9.26: Block diagram of Class D amplifier

9.10 AMPLIFIER EFFICIENCY SUMMARY

The power efficiency of an amplifier, defined as the ratio of power output to power input, improves (gets higher) going from class A to class D. In general terms, we see that a *class A* amplifier, with dc bias at one-half the supply voltage level, uses a good amount of power to maintain bias, even with no input signal applied. This results in very poor efficiency, especially with small input signals, when very little ac power is delivered to the load. In fact, the maximum efficiency of a class A circuit, occurring for the largest output voltage and current swing, is only 25% with a direct or series-fed load connection and 50% with a transformer connection to the load. *Class B* operation, with no dc bias power for no input signal, can be shown to provide a maximum efficiency that reaches 78.5%. c*lass D* operation can achieve power efficiency over 90% and provides the most efficient operation of all the operating classes. Since *class AB* falls between class A and class B in bias, it also falls between their efficiency

ratings—between 25% (or 50%) and 78.5%. Table 9.1 summarizes the operation of the various amplifier classes. This table provides a relative comparison of the output cycle operation and power efficiency for the various class types. In *class B* operation, a push-pull connection is obtained using either a transformer coupling or by using complementary (or quasi-complementary) operation with npn and pnp transistors to provide operation on opposite polarity cycles. While transformer operation can provide opposite cycle signals, the transformer itself is quite large in many applications. A transformerless circuit using complementary transistors provides the same operation in a much smaller package.

			Class		
	A	AB	B	C*	D
Operating cycle	360°	180° to 360°	180°	Less than 180°	Pulse operation
Power efficiency	25% to 50%	Between 25% (50%) and 78.5%	78.5%		Typically over 90%

- Class C is usually not used for delivering large amounts of power, thus the efficiency is not given here.

Table 9.1 Comparison of Amplifier Classes